MICRO ELECTRONICS

PROGRAMMABLE TV GAMES

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NO.
GIMINI CHALLENGER "8950" PROGRAMMABLE GAME SYSTEM	BASIC COMPONENTS: A complete microprocessor programmable game with only 3 LSI chips (plus standard RAM), the GIMINI Challenger "8950" is ideal for sports games and games of chance and mental skill.	CP1610	7-86
		AY-3-8950	7-78
		AY-3-8950-1	7-78
		RO-3-9501	7-92
		2112A	7-99
	OPTIONAL COMPONENTS: The basic "8950" system can be expanded to include additional ROM and RAM, and to add complex sound generation.	RO-3-9500	7-92
		2112A/2114	7-99
		AY-3-8910	7-100
GIMINI DELUXE "8900" PROGRAMMABLE GAME SYSTEM	BASIC COMPONENTS: A complete microprocessor programmable game with only 5 LSI chips, the GIMINI Deluxe "8900" offers the capability for maximum game flexibility with detailed graphics definition and manipulation.	CP1610	7-107
		AY-3-8900	7-107
		AY-3-8900-1	7-107
		RO-3-9502	7-108
		RO-3-9503	7-108
		RA-3-9600	7-108
	OPTIONAL COMPONENTS: The basic "8900" system can easily be expanded to include additional games plus software-controlled graphics interaction, complex sound generation, and supplementary peripherals.	RO-3-9500	7-109
		2112A/2114	7-109
		AY-3-8910	7-109
		AY-3-8915	7-109
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GIMINI Challenger "8950" Programmable Game Set

FEATURES

- User game design capability
- Completely software programmable
- Extensive game library availability in addition to custom software development
- Versatile game instruction set
- NTSC compatible T.V. sync generator
- Color circuitry
- Software controlled score and playfield placement capability

DESCRIPTION

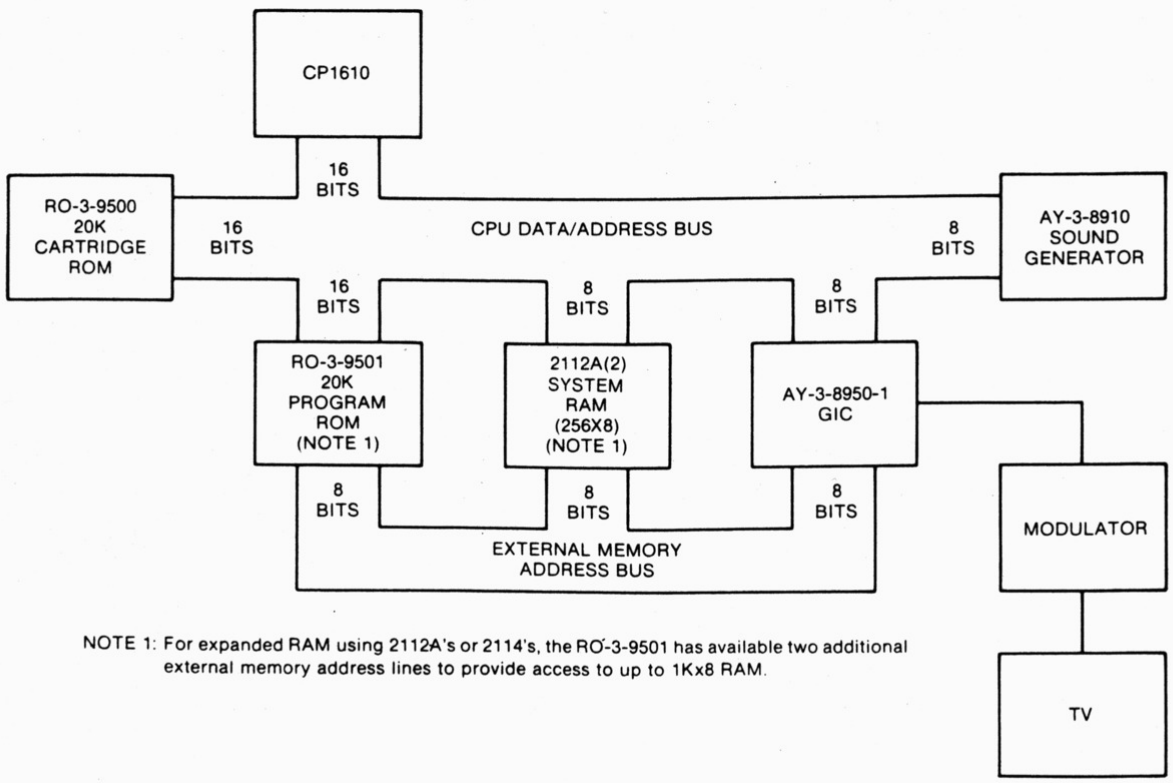
The GIMINI Challenger "8950" Programmable Game Set is a multichip set which can accept different programming ROMs, programmed by the user or available form our extensive game library. The Game Set provides an unlimited number of games; including aggression games, racing games, gambling games, etc. The set consists of the CP1610 microprocessor, a 20K resident ROM game program chip (RO-3-9501), two user-supplied 256 × 4 static RAMs (2112A), and the AY-3-8950-1 graphics interface circuit. Cartridge ROMs (RO-3-9500) extend the user's game options, and the AY-3-8910 Programmable Sound Generator provides game sound effects as well as I/O ports for the game control units.

The GIMINI "8950" system has been desinged as a minimum chip system which provides a very cost-effective and flexible solution to programmability. Since the architecture of the system is based on the CP1610 microprocessor, not only are variations of games limitless, but an endless variety of functions beyond a "game" function are possible.

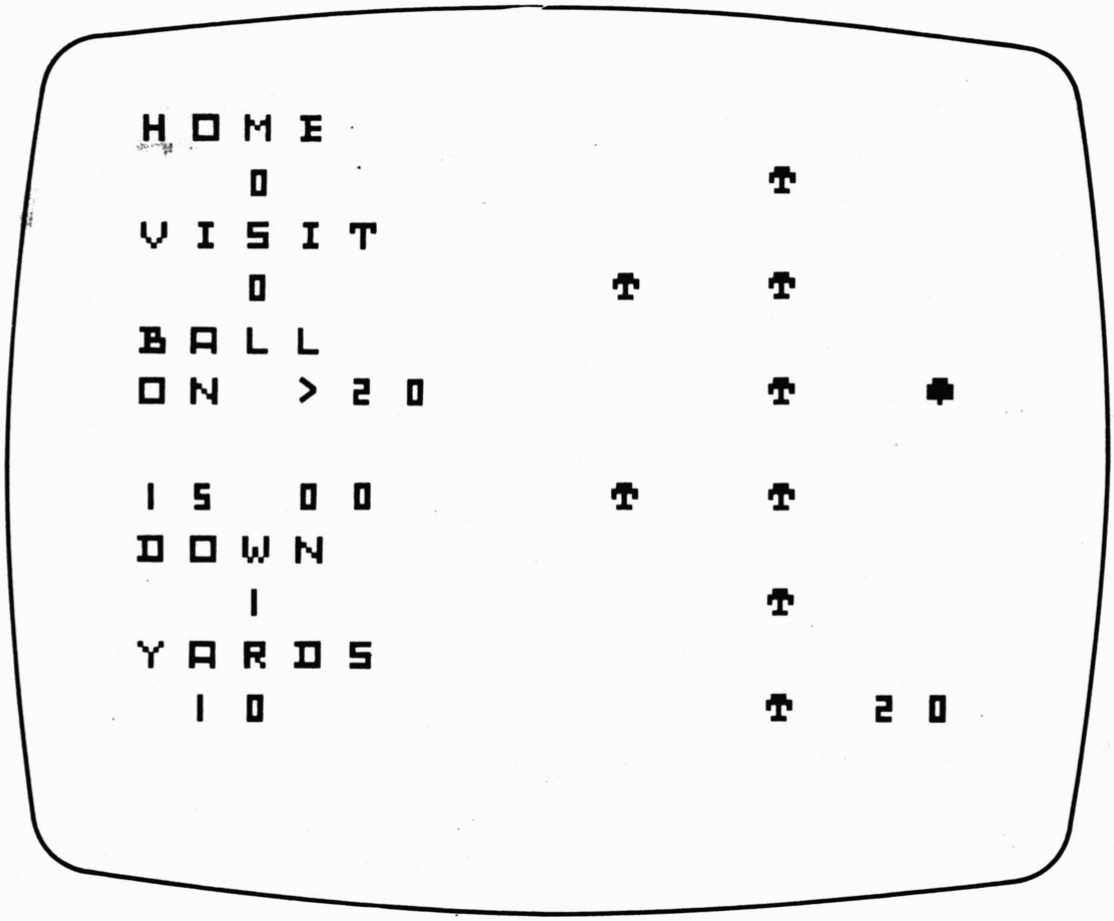
The GIMINI "8950" system is supported by an extremely flexible emulator/development system which provides the capability for a manufacturer to develop and generate new games and to demonstrate these games prior to committing the game program to ROM.

Full details on the GIMINI "8950" system components are contained in the data sheets in this section.

SYSTEM DIAGRAM



NOTE 1: For expanded RAM using 2112A's or 2114's, the RO-3-9501 has available two additional external memory address lines to provide access to up to 1Kx8 RAM.



Computer Mini Football Cartridge

It's you against a friend with the computer controlling the defense.

Start the game by pushing "YES" when "PRO" or "SEMI PRO" appears to choose the strength of the defense. Player one is the Home team (Clubs) and defends the left goal. Player two is the Visiting team (Spades) and defends the right goal.

Try to make ten yards in four carries by moving your offensive player according to the arrows on the control. You may leave your direction control depressed and let the computer move for you, or keep pushing and releasing the button to move faster.

The computer controls the six line men and two defensive backs and is programmed to tackle you. When you are tackled, the player responsible flashes and the crowd roars.

The screen shows thirteen yards and is set up at the beginning of the play with three yards behind you and ten ahead, and the ball on the line of scrimmage. If you run past all of the defenders, the computer "pans" the field ahead thirteen yards and watches you enter from the other end. If you make at least ten yards in four downs or less, you are given a "first and ten" where the ball was downed.

On fourth down you may elect to kick by pushing "yes" or continue the fourth down play by pushing "no". The computer randomly controls the distance of the kick and the run back. If the ball passes between the goal posts, you get a three point filed goal. If the ball is turned over to the other team, their fight song is played.

If you evade all of the defenders and cross the "G" goal line, you are awarded seven points and the computer plays "charge". If you are caught in your own end zone, your opponent is given two points and the ball.

The game has four quarters of fifteen "mini-minutes" each. At two minutes before half time and the end of the game, a two minute warning is given.

Strategy Cartridge

Strategy is a 1-4 player dice game. If less than 4 players are selected, the computer may also play against the other players. The object of the game is to accumulate the highest score possible on your score card. The score card consists of 13 categories and a bonus section. The categories are as follows: ones, twos, threes, fours, fives, sixes, three of a kind, four of a kind, full house, small straight (i.e. 1, 2, 3, 4), large straight (i.e. 1, 2, 3, 4, 5), chance, and stragety (five of a kind).

Points are scored by rolling five dice (computer simulated) and totalling the resulting score in an unused category on your card. Players take turns "rolling dice" and scoring points until every category on the score card is filled. At the end of the game, scores are automatically totalled and displayed. Each player's turn consists of up to 3 rolls of the dice from 1 to 5 dice. Scoring for the categories is as follows:

Ones = Total of dice equal to 1
Twos = Total of dice equal to 2
Threes = Total of dice equal to 3
Fours = Total of dice equal to 4
Fives = Total of dice equal to 5
Sixes = Total of dice equal to 6
3 of a Kind = Total of the 3 dice (3 sixes = 18)
4 of a Kind = Total of the 4 dice
Full House = 25
Small Straight = 30
Large Straight = 40
Chance = Total of all dice
Strategy = 50

One hundred bonus points are scored for every "strategy" after the first one.

Spellbound Cartridge

Spellbound is a word game in which each of two players, in turn, is randomly dealt a "tray" of seven letters, on screen, by the computer. Using his control-unit, player #1, may elect to either form a word or discard any two of his letters when the message "DISCARD?" is displayed. If player #1 so chooses, he may discard by operating his "YES" button which causes the first (left-most) letter of his "tray" to flash. Operation of the "NO" button causes the next letter to flash and he may now decide to discard or retain it. This sequence continues until he has chosen two letters to discard. (The computer will provide two additional random letters after the second player's turn). After player #1's second discard, control reverts to player #2, who may elect to form a word or discard.

Points are awarded based on the letters used and their relative positions. The computer randomly assigns letter and word multipliers for each round, keeping track of each player's score and displaying them in the upper left of the screen. In the example above, using a "Z" over the X3 awards 30 points instead of the single letter value of 10 for "Z". The word multiplier is also random and may be "SINGLE", "DOUBLE" or "TRIPLE". It appears in the lower left of the screen. In the example above, the word "BUZZARD" has a "DOUBLE" word score of 106 points. Prior to awarding the point value, the opposing player is asked to verify the assembled word. Upon verification, the player's score is adjusted and he is given the opportunity of discarding two of the letters in the assembled word. These two letters are replaced, randomly, by the computer after the opponent has concluded his round. The first player to accumulate 200 points wins the game.

Jumble Cartridge

Jumble is a variation of the popular scrambled letters word guessing game. Words can be from four through six letters which are selected and jumbled by the computer randomly. Should the same word be selected by the computer at another time, it is likely to have the letters jumbled in a different order. The first player to unscramble the jumbled word will be awarded a variable number of points, with more points awarded for an early guess. The first player to reach ten points wins the game.

Hangman Cartridge

The object of Hangman is to guess a mystery word that the computer has chosen. The computer uses a 300 word dictionary comprised of 100 four-letter, 100 five-letter, and 100 six-letter words. At the start of the game, the computer displays the alphabet and 4, 5, or 6 dashes to indicate how many letters are in the mystery word. The player then selects a letter from the alphabet. If the chosen letter is in the mystery word, it is displayed in the correct position(s) and play continues. For every wrong letter guess, a different portion of a "man" is displayed on the left portion of the screen. Play continues until the mystery word is correctly spelled or until the "man" is completely displayed. Six wrong guesses will "hang the man."

Astrowar Cartridge

An enemy warship has sent 3 nuclear torpedoes directed for destruction of your vessel. Your only means of survival is destroyinrpedoes before they reach you. The only means of determining their exact location is thru magnetic directors. A salvo of 3 are launched in the direction of an incoming torpedo. When the directors pass by the incoming torpedo, a computer readout gives the sum of the (X, Y) coordinates of the distance of the miss. After the 3 "sums of the coordinates" are given, a determination must be quickly made on the exact location of the torpedo, and the torpedo destroyed before it reaches the vicinity of your vessel (a time-to-impact readout is given). All 3 torpedoes must be destroyed, one after the other.

If this is accomplished, your vessel goes on the offensive and you must destroy the enemy warship before he fires another salvo of torpedoes.

The game goes on and on until an enemy torpedo destroys your starship (a lose message is displayed), or the enemy is destroyed (a win message is displayed).

Battleship Cartridge

This game is played on a 13X5 matrix displayed on the TV screen as "A" thru "M" horizontally and "1" thru "5" vertically. Ships consist of 1 to 5 horizontal units: aircraft carrier = 5, battleship = 3, destroyer = 2, submarine = 1. 1 aircraft carrier, 2 battleships, 2 destroyers, and 4 subs are randomly placed invisibly in the matrix area. The game is initially played with 45 torpedoes. The player selects an area by a coordinate pair of digits and fires his torpedoes one at a time. A miss is recorded by placing a dash in the appropriate location on the screen; a hit places a zero. To win the game, all locations of a ship, and all ships must be hit before running out of torpedoes. A win message is displayed. If the player runs out of torpedoes before the last ship is totally destroyed, the game is over and a loss message is displayed.

The following games introduce a new factor only possible with "computer" games. The computer actually "learns" by playing to effectively become a more skilled opponent.

Awari Cartridge

You play against a modern computer at the world's oldest game. In ancient days, the game was played using pebbles in pits in the ground. Your computer shows the number of pebbles in the pits with a number. The computer plays on the black squares and you play on the red.

The rules are simple. You pick up all of the pebbles in a pit and deposit them one at a time into the following pits, going counter clockwise. If the last beam drops into the scoring pit on the right side of the screen, you get one more turn. If the last bean falls into an empty pit, the computer moves it and the pebbles in the pit acress from it into the scoring pit (if the other pit is not empty).

The game begins when you answer "yes" or "no" when asked if you want to make the first move.

The game is over when you or the computer have no pebbles left in the playing pits. You win if you have more pebbles in your scoring pit. The computer offers legal moves by placing an arrow over the pit. A "yes" will begin the move, and a "no" will advance to the next legal move.

Be careful - as you gain in skill, the computer is programmed to begin playing more intelligently.

Nim Cartridge

Nim is a game of logic where the player who takes the last piece wins.

If you allow the computer to set up the board, it will randomly set from one to six rows of from one to thirteen pieces. You are allowed to set up the board by choosing the number of rows with variable number of pieces in each row.

Since the player who goes first has an advantage, the computer flips a coin and allows you to call heads by pressing "yes" and tails by pushing "no". If our choice comes up, you may choose to go first by pushing "yes" when the computer asks.

When it is your turn, you first choose the row by pushing "no" until the proper row is chosen, then "yes". Once you have chosen a row, each depression of "yes" takes another piece until the "no" is pushed or all pieces are gone.

As with Awari, the computer gets "smarter" if you beat it often enough.

Tic Tac Toe Cartridge

Similar to the conventional game, but computer learns through successive plays.

Hex Pawn Cartridge

The game is played on a 3×3 grid, each player (you and the computer) has 3 pawns on his side of the grid. The pawns move in a similar manner to chess. The program learns by elimination of bad moves. This successfully makes the machine a better opponent. The philosophy behind this game leads to other cybernetic games in which the computer "learns" as it plays.

Even—Cybernetics Game Cartridge

An odd number of objects is placed in a row. You take turns with the computer picking up between one and four objects each turn. The game ends when there are no objects left, and the winner is the one with an even number of objects picked up. The computer starts out only knowing the rules of the game. Using techniques of artificial intelligence, it gradually learns to play from its mistakes until it plays a very good game. After approx. 20 games, the computer is a challenge to beat.

Munch Cartridge

Game for 1-4 players on a 12 (horizontal) × 5 (vertical) grid. A poison "P" square is positioned in the upper left-hand of the cookie grid. Each player, in turn, munches a piece of the cookie avoiding the poison square. To munch the cookie, the player selects a row and column after which all the squares on the row and column selected and the squares below and to the right of the selection disappear. The victor is the player that survives.

Graphics Interface

FEATURES

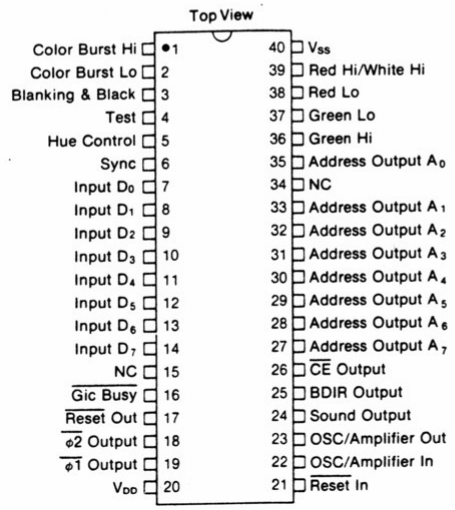
- On-chip 64 character generator ROM
- On-chip oscillator/amplifier
- Direct interface to CP1610, RO-3-9500 Series ROMS, 2112A/2114 Series RAMS, and AY-3-8910 Programmable Sound Generator.
- On-chip NTSC compatible T.V. sync generator
- On-chip color circuitry

DESCRIPTION

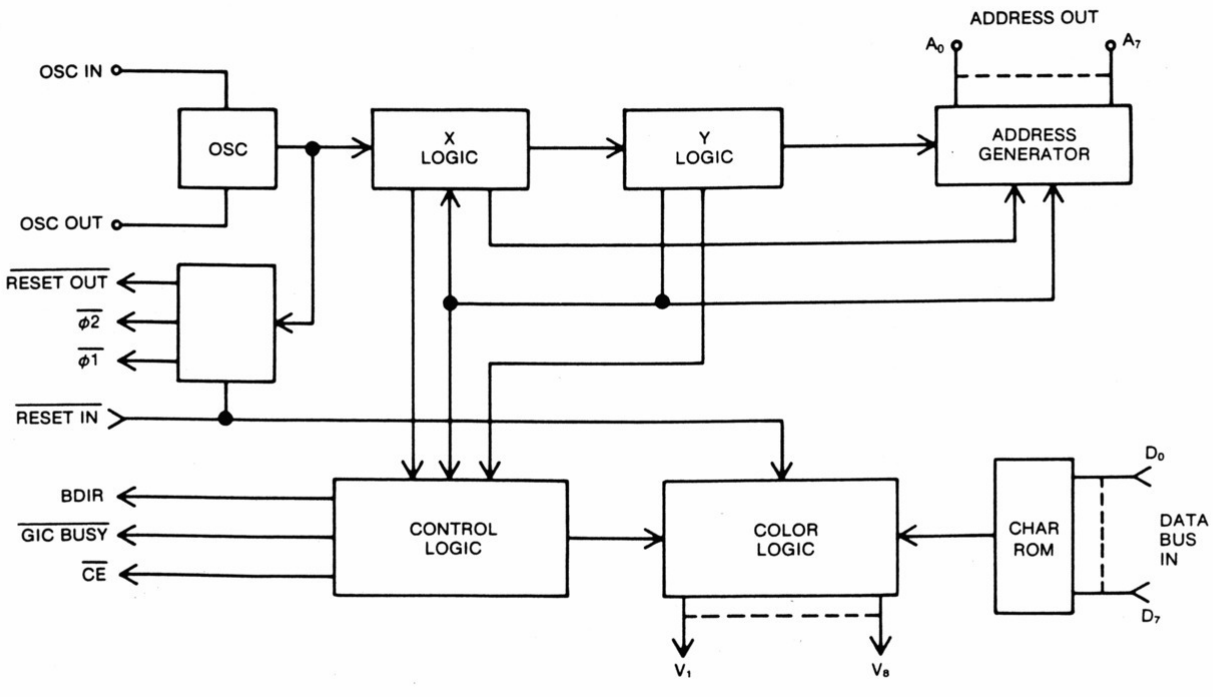
The AY-3-8950-1 Graphics Interface Chip (GIC) is the T.V. display generator for the GIMINI "Challenger" programmable game system. The GIC reads the contents of the RAM, decodes it and displays the requested information on a standard 525 line T.V. The GIC provides the complete T.V. signal including sync, color burst, blanking and video data.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



BLOCK DIAGRAM



PIN FUNCTIONS

Pin	Name	Function
10 VIDEO PINS:		
36	Green Hi	This is an open drain output device to V_{SS}. It is low impedance whenever green is to be displayed. It is high impedance otherwise.
37	Green Lo	This is an open drain output device to V_{SS}. It is low impedance at a 3.58 MHz rate when green is selected. It is high impedance otherwise.
39	Red Hi/White Hi	This has two open drain output devices to V_{SS}. It is low impedance whenever red or white is to be displayed. White and red are never on together. When white is to be displayed, the output reaches voltage V_{OUT} 1. When red is to be displayed the output reaches voltage V_{OUT} 2 which is a different voltage level than V_{OUT} 1.
3	Black/Blanking	This has two open drain devices similar to Pin 39. One device is on when black is to be displayed. The other is on when blanking is displayed.
38	Red Lo	This is an open drain device to V_{SS} similar to green lo.
1	CBH-Color Burst Hi	This is an open drain device to V_{SS} similar to Pins 36 and 39.
2	CBL-Color Burst Lo	This is an open drain device to V_{SS} similar to Pins 36, 39 and 1. It is identical to Pin 39 because there are two output devices connected to this pin. Only one output device can be on at one time.
6	Sync	This is an open drain device to V_{SS} similar to Pins 36, 39, 1 and 3.
4	Test	This input disables the 3.58 MHz from appearing on the color outputs. There is an internal pull down on this input.
5	Hue Control	This input changes the phase of the 3.58 MHz on the color outputs.
8 DATA INPUTS:		
7-14	D0-D7	These are inputs to the ROM section of the GIC. The 8 bit input is decoded into 1 of 64 alphanumeric characters or special characters. There is a pull-up resistor of 5K ohms on each input. The 64 alphanumeric characters are shown in Appendix A. To select character inputs D6 and D7 must be zero. Alphanumeric

	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	6	BIT	OCTAL	CODE		
PINS	14	13	12	11	10	9	8	7

EXAMPLES:

LETTER "G"	0	0	0	0	0	1	1	1
NUMBER "5"	0	0	1	1	0	1	0	1

TO SELECT A SPECIAL CHARACTER MAKE D6 = 1

0	1	6	BIT	OCTAL	CODE

EXAMPLES:

EX. 1	0	1	1	1	1	0	1	1
EX. 2	0	1	1	0	1	1	1	0

THE CODES TO SELECT SPECIALS ARE SHOWN IN APPENDIX B.

8 ADDRESS OUTPUTS:		
35, 33-27	A0-A7	These are outputs from the GIC to the RAM. They address the RAM to produce the 8 bit word for the data input Pins 7-14. To put a character in a particular place on the screen, write the code number into the appropriate RAM address. The location of the data on the screen is shown in Appendix D. To display a G, write the code 00000111 into RAM location 164 as shown in Appendix "C". The outputs addressing the RAM are push-pull.

TV GAMES

PIN FUNCTIONS (continued)

Pin	Name	Function
4 SYSTEM OUTPUTS:		
16	$\overline{\text{GIC Busy}}$	This is a push-pull output. It goes low at line 46 and high at line 240.
25	BDIR	This is a push pull output. It goes high at line 47 from X position 50 to X position 86 for each frame.
26	$\overline{\text{CE}}$	This is an open drain single device to Vss. It goes low at line 48 and remains low until line 240 when it returns to high.
24	Sound	This is a push-pull output. It is low when there is no sound. When sound is selected the output is 2kHz. 1kHz or 500 Hz depending on the data in RAM location 226. D0 in loc. 226 selects 2kHz, D1 in loc. 226 selects 1kHz and D2 selects 500 Hz. The sound lasts for the duration of the data bits in RAM location 226.
6 CLOCKS AND RESETS I/O:		
23	Osc. Input	This is a hi-impedance input to the oscillator. Osc. freq. is 3.579545 MHz.
22	Osc. Output	This is the output of the internal oscillator amplifier.
19	$\overline{\phi 1}$ Output	These 2 pins are push-pull outputs which drive the CPU clock generators at one-half of the osc. freq.
18	$\overline{\phi 2}$ Output	
21	$\overline{\text{Reset}}$ In	This input resets the GIC sync generator. The osc. is not affected. ϕ 1 is reset Hi, ϕ 2 low, M sync out low, GIC Busy Hi, BDIR low, CE hi, Sound is not determined, address outputs are hi impedance, and color outputs are off.
17	$\overline{\text{Reset}}$ Out	This output to the CPU is a push-pull signal.

ELECTRICAL CHARACTERISTICS

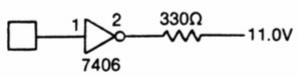
Maximum Ratings*

V_{DD} ..... -0.3 to +12.0V
Storage Temperature ..... -20° C to +70° C

*Exceeding these ranges could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

STANDARD CONDITIONS (unless otherwise noted)

V_{DD}=5.0V ± 5%
V_{SS}=0.0V
Ambient Temperature=0° C to +40° C

Characteristic	Min.	Typ.**	Max.	Units	Conditions
Clock Frequency	–	3.579	–	MHz	Std. color crystal
Input Logic Levels					
Logic 0	0.0	–	0.5	V	
Logic 1	3.5	–	V_{DD}	V	
I_{DD}	–	–	125	mA	@ 5V
Input Currents					
Data Inputs D0-D7	-0.3	–	-4.0	mA	Input connected to V_{SS}
Master Clear Input	-0.1	–	-1.3	mA	Input connected to V_{SS}
Test Input	30	–	400	μA	Input connected to V_{DD}
Address Outputs					2.7K Ω to V_{DD}
Logic 0	0.0	–	1.0	V	
Logic 1	3.0	–	V_{DD}	V	
Output current in high imped. state	-0.15	–	-2.0	mA	Out. connected to V_{SS} Reset pin at gnd.
System Outputs					
$\overline{\phi 1}$, $\overline{\phi 2}$					
Logic 0	0.0	–	1.0	V	
Logic 1	3.0	–	V_{DD}	V	
BDIR, $\overline{\text{GIC BUSY}}$, Sound					
Logic 0	0.0	–	1.0	V	2.7K to V_{DD}
Logic 1	3.0	–	V_{DD}	V	
$\overline{\text{CE}}$ open collector output					
Logic 0	0.0	–	1.0	V	2.7K to V_{DD}

SYSTEM OPERATION

The System Diagram is shown below. During the time the GIC busy signal is high, the CP 1610 is operating to make game and display computations. The 20K ROM supplies the instructions to the CP 1610. The RAM locations 227-377 (octal) provide scratch pad memory for the CP 1610. The address code in GIC ROM of the character to be displayed is written into the appropriate RAM locations by the CP 1610.

When the GIC busy signal goes low the CP1610 stops all computations and goes into a waiting mode. The GIC chip then reads the RAM to determine what is to be displayed on the T.V. The GIC automatically formats the T.V. screen as shown in Appendix D. Each of the first 225 (octal) RAM Locations corresponds to specific T.V. picture slots as shown. For example, the code for the letter "G" (00000111) when placed in RAM location 164_8 causes the "G" to appear on the T.V. screen in slot 164_8.

Alphanumeric characters can be written in any screen slot as shown in Appendix E. In addition, special characters can be displayed on the right hand side of the T.V. screen as shown in Appendix F.

When the GIC chip stops accessing the RAM, the GIC busy signal goes high again. The CP 1610 goes out of the waiting mode and resumes its computations from where it left off. The CP 1610 computes for 4 millisec out of every 16 millisec available.

SYSTEM ORGANIZATION

When the GIC busy signal is high, the external address bus and data bus are controlled by the CPU and the status of these buses is indicated by BC1, BC2 and BDIR.

AY-3-8950-1 OPERATION

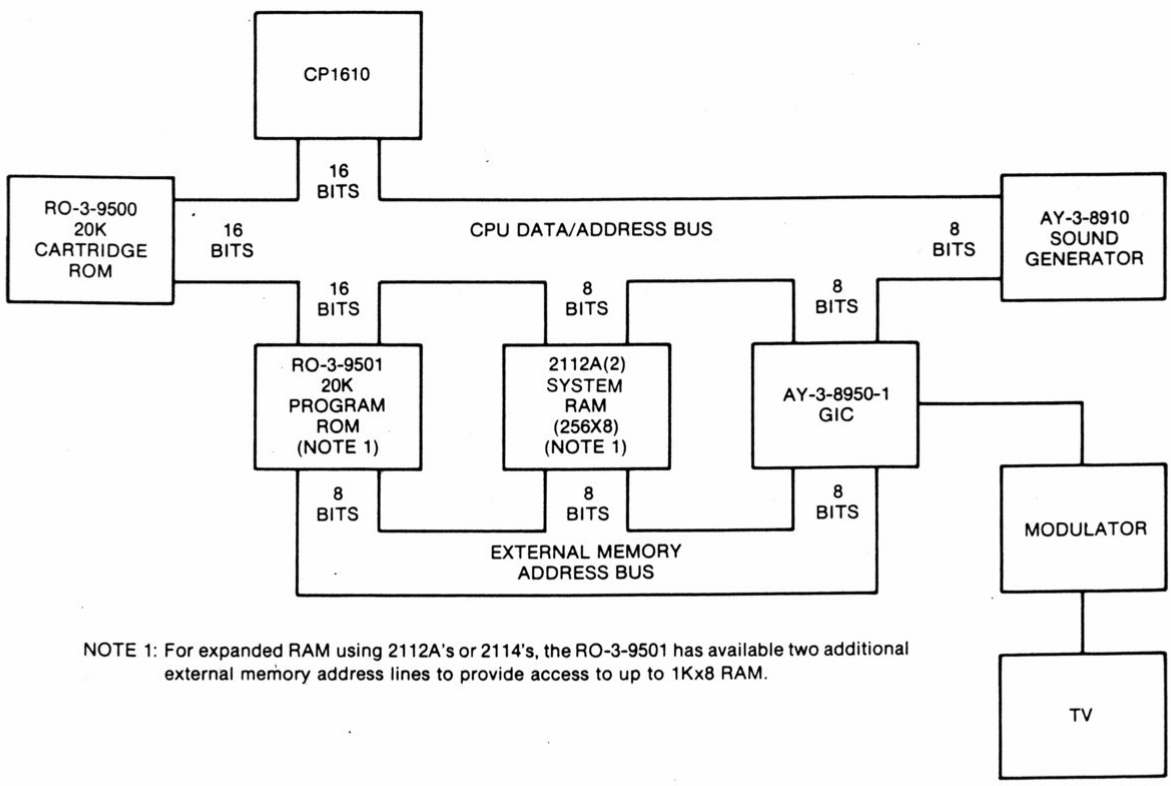
The GIC can display alphanumeric messages on the T.V. as shown in Appendix E. The character set is shown in Appendix A. The characters include the most widely used Alphanumerics.

To write the message in Appendix E, the CPU has placed the following codes in the RAM.

LOC (Octal)	Data (Octal)	T.V. Symbol
111	0024	T
112	0010	H
113	0005	E
114	0000	Space
		Etc.

The GIC automatically reads the RAM in the proper sequence. The data from the RAM addresses the internal GIC character generator ROM. The resultant data is loaded into register and shifted out.

SYSTEM DIAGRAM



NOTE 1: For expanded RAM using 2112A's or 2114's, the RO-3-9501 has available two additional external memory address lines to provide access to up to 1Kx8 RAM.

RULES OF GIC SYSTEM VIDEO OUTPUT

The left side of screen can display 64 alphanumeric symbols contained in memory on boxes arranged 6 across and 12 down. The 5 x 7 characters are placed on the 6 x 8 boxes to provide spacing between them. The characters are white on a green background. (See Appendix A)

The right side of the screen can display any one of the 64 alpha numeric characters 5 x 7 in size on the bottom portion of the 9 x 16 boxes arranged 13 across and 6 down. The characters are white on a green background. (See Appendix A)

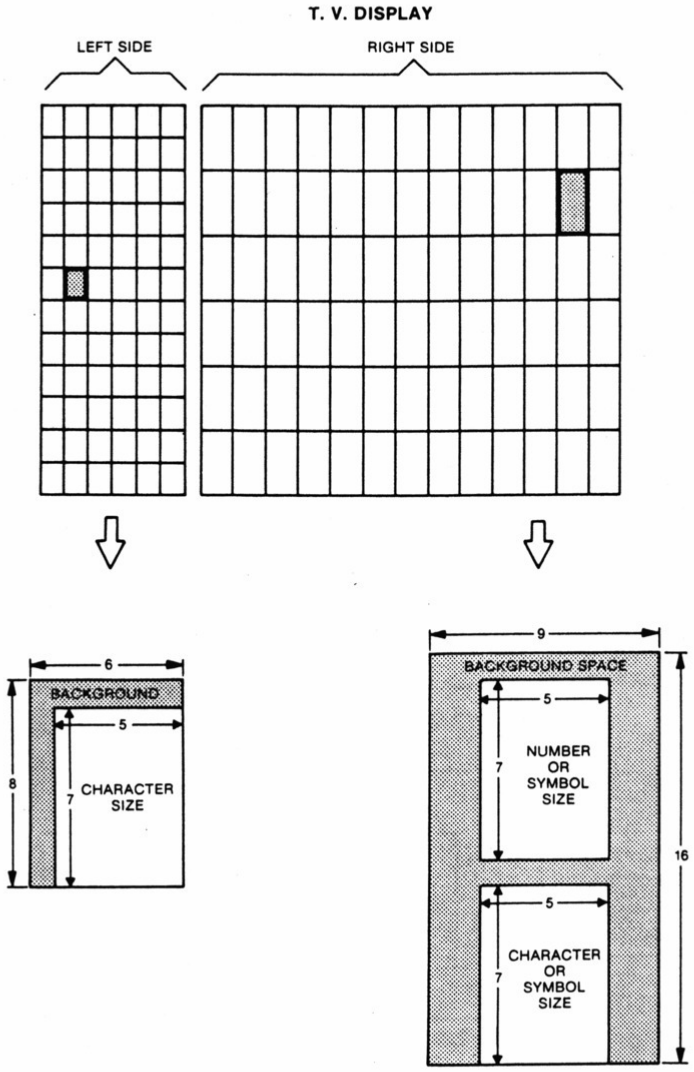
OR

The right side of the screen can display the numbers 0 to 10, J, Q, K, and A on the top portion of the 9 × 16 boxes. The bottom portion can display a club, a diamond, a spade, or a heart only. (See Applendix B)

The character chosen for the bottom portion of the box determines the background color for the entire box. A club or a spade specifies a black box while a diamond or a heart specifies a red rectangle. All characters are displayed as white.

OR

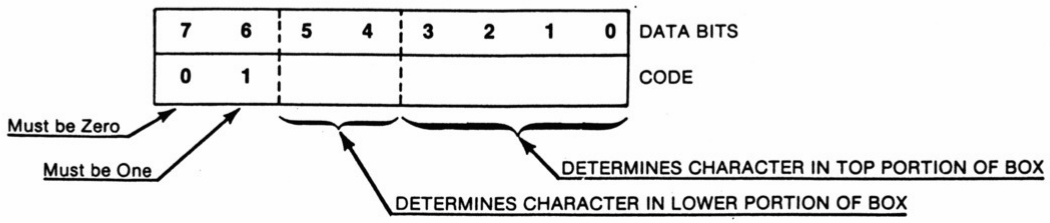
The right side of the screen can display a white output for the full size of the 9 x 16 box when chosen.



APPENDIX A: Alphanumeric Shapes

Code	Character	Code	Character	Code	Character	Code	Character
00	Space	20	P	40	Space	60	0
01	A	21	Q	41	!	61	1
02	B	22	R	42	"	62	2
03	C	23	S	43	#	63	3
04	D	24	T	44	$	64	4
05	E	25	U	45	%	65	5
06	F	26	V	46	&	66	6
07	G	27	W	47	'	67	7
10	H	30	X	50	)	70	8
11	I	31	Y	51	(	71	9
12	J	32	Z	52	:	72	10
13	K	33	↓	53	+	73	J
14	L	34	Club	54	-	74	Q
15	M	35	Diamond	55	=	75	K
16	N	36	Spade	56	.	76	A
17	O	37	Heart	57	÷	77	?

APPENDIX B: Color Mode Right Hand Screen



DATA IN UPPER RECTANGLE

Data Bits 3	2	1	0	Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	J
1	1	0	0	Q
1	1	0	1	K
1	1	1	0	A
1	1	1	1	?

DATA IN LOWER RECTANGLE

Data Bits 5	4	Character
0	0	Club - BLACK
0	1	Diamond - RED
1	0	Spade - BLACK
1	1	Heart - RED

7	6	5	4	3	2	1	0	
1	1	–	–	–	–	–	–	CODE

DATA BITS

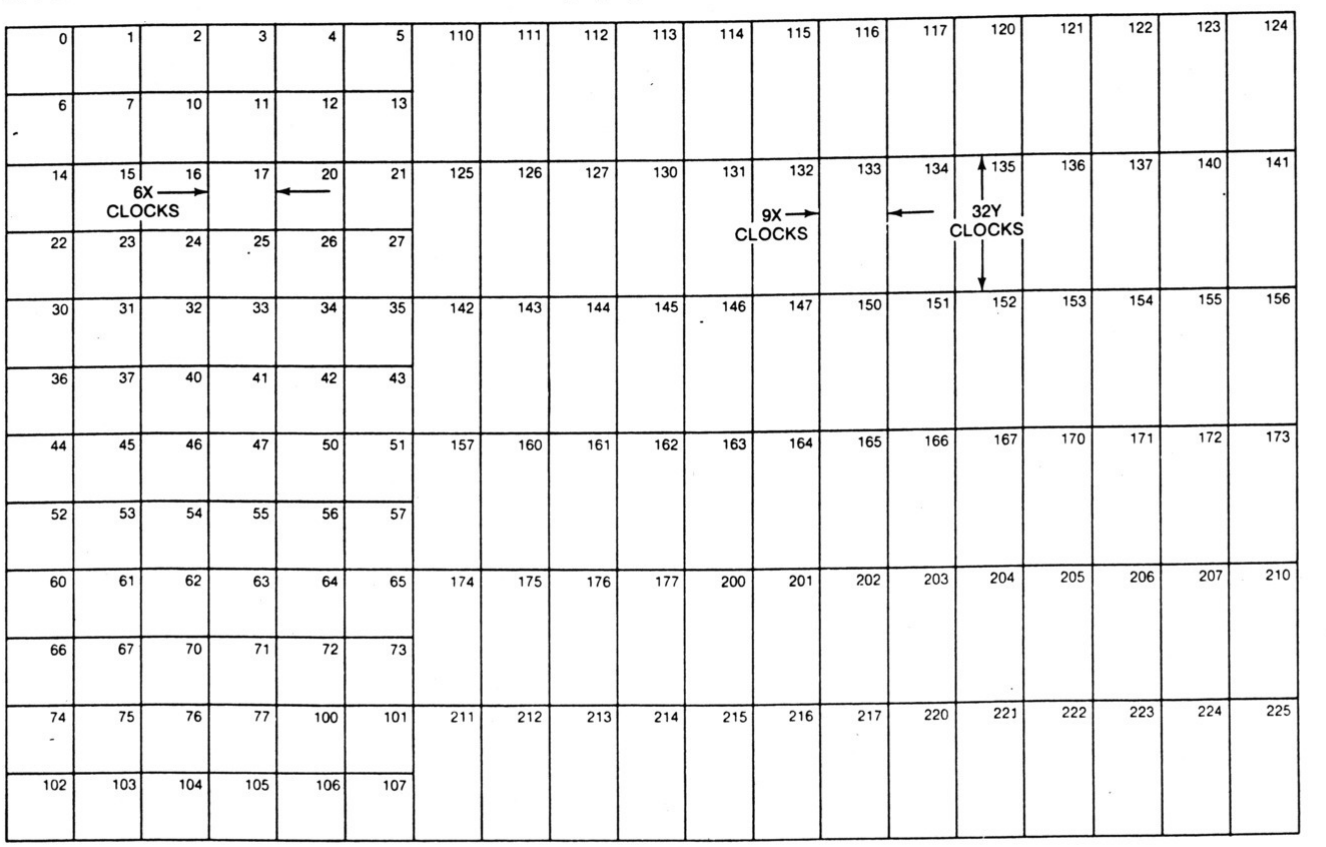
This code causes the entire rectangle to be white.

TV GAMES

APPENDIX C Chart for Programming RAM

LOC	Data	LOC	Data	LOC	Data	LOC	Data	LOC	Data	LOC	Data	LOC	Data
0		30		60		110		140		170		220	
1		31		61		111		141		171		221	
2		32		62		112		142		172		222	
3		33		63		113		143		173		223	
4		34		64		114		144		174		224	
5		35		65		115		145		175		225	
6		36		66		116		146		176			
7		37		67		117		147		177			
10		40		70		120		150		200			
11		41		71		121		151		201			
12		42		72		122		152		202			
13		43		73		123		153		203			
14		44		74		124		154		204			
15		45		75		125		155		205			
16		46		76		126		156		206			
17		47		77		127		157		207			
20		50		100		130		160		210			
21		51		101		131		161		211			
22		52		102		132		162		212			
23		53		103		133		163		213			
24		54		104		134		164	00000111	214			
25		55		105		135		165		215			
26		56		106		136		166		216			
27		57		107		137		167		217			

APPENDIX D: Octal Location of RAM Addresses Display by GIC



226-SOUND 277 – 377 - SCRATCH (CPU)

APPENDIX E: AY-3-8950-1 Display RAM Layout

ALPHANUMERICS

0 T	1 H	2 E	3 S	4 E	5	110	111 T	112 H	113 E	114	115 G	116 I	117 C	120	121 C	122 A	123 N	124
6 C	7 A	10 N	11	12	13													
14 A	15 L	16 S	17 O	20	21	125 D	126 I	127 S	130 P	131 L	132 A	133 Y	134	135 6	136 4	137	140	141
22 B	23 E	24	25	26	27													
30 S	31 H	32 O	33 W	34 N	35	142 A	143 L	144 P	145 H	146 A	147 N	150 U	151 M	152 E	153 R	154 I	155 C	156
36	37	40	41	42	43													
44 $	45 $	46 $	47 %	50 %	51 %	157	160 C	161 H	162 A	163 R	164 A	165 C	166 T	167 E	170 R	171 S	172	173
52 +	53 +	54 +	55 —	56 —	57 —													
60 •	61 •	62 •	63 /	64 /	65 /	174	175	176	177	200	201	202	203	204	205	206	207	210
66	67	70	71	72	73													
74 E	75 T	76 C	77 •	100	101	211	212	213	214	215	216	217	220	221	222	223	224	225
102	103	104	105	106	107													

226-SOUND 277 → 377 - SCRATCH (CPU)

APPENDIX: E: AY-3-8950-1 Special Characters

ALPHANUMERICS

0	1	2	3	4	5	110	111	112 GREEN BACKGROUND	113	114	115	116	117	120	121	122	123	124
6	7	10	11	12	13													
14	15	16	17	20	21	125	126	127	130	131	132	133	134	135	136	137	140	141
22	23	24	25	26	27													
30	31	32	33	34	35	142	143	144 J ◇ RED	145	146 7 ◇ RED	147	150	151	152	153	154 K ♠ BLACK	155	156
36	37	40	41	42	43													
44	45	46	47	50	51	157	160	161 2 ♣ BLACK	162	163 A ◇ RED	164	165 K ♣ BLACK	166	167	170	171	172	173
52	53	54	55	56	57													
60	61	62	63	64	65	174	175	176	177	200	201	202	203	204	205	206	207	210
66	67	70	71	72	73													
74	75	76	77	100	101	211	212	213	214	215	216	217	220	221	222	223	224	225
102	103	104	105	106	107													

226-SOUND 277 → 377 - SCRATCH (CPU)

TV GAMES

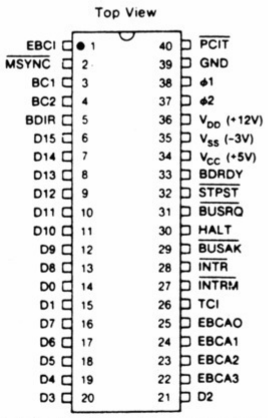
16-Bit Single-Chip Microprocessor

FEATURES

- 8 program accessible 16-bit general purpose registers
- 87 basic instructions
- 4 addressing modes: immediate, direct, indirect, relative
- Conditional branching on status word and 16 external conditions
- Unlimited interrupt nesting and priority resolution
- 16-bit 2's complement arithmetic & logic
- Status word: carry, overflow, sign, zero
- Direct memory access (DMA) for high speed data transfer
- 64K memory using single address
- TTL compatible/simple bus structure
- 1 μs cycle time, 2 MHz 2-phase clock

PIN CONFIGURATION

40 LEAD DUAL IN LINE



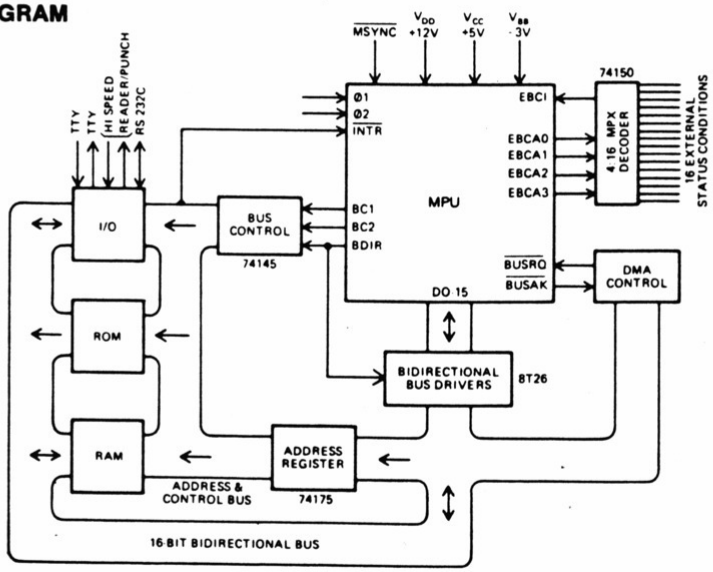
DESCRIPTION

The CP1610 is a compatible member of the Series 1600 Microprocessor products family. It is a complete, 16-bit, single chip, high speed MOS-LSI Microprocessor. The Series 1600 family is fabricated with General Instrument's N-Channel Ion-Implant GIANT II process, insuring high performance with proven reliability and production history. All members of the Series 1600 family, including Programmable Interface Controllers, Read Only Memories, and Random Access Read/Write Memories are fully compatible with the CP1610.

The Microprocessor has been designed for high speed data processing and real time applications. Typical applications include programmable TV games, home computer systems/ home information centers, programmable calculator systems, peripheral controllers, process controllers, intelligent terminals and instruments, data acquisition and digital communications processors, numerical control systems and many general purpose mini-computer applications.The Microprocessor can readily support a variety of peripheral equipment such as TTY, CRT display, tape reader/punch, A/D & D/A converter, keyboard, cassette tape, floppy disk, and RS-232C data communication lines.

The CP1610 utilizes third generation minicomputer architecture with eight general purpose registers to achieve a versatile, sophisticated microcomputer system. The 16-bit word enables fast and efficient processing of alphanumeric or byte oriented data. The 16-bit address capability permits access to 65,536 words in any combination of program, memory, data memory, or peripheral devices. This single address space concept, combined with a powerful instruction set and microprogrammable Peripheral Interface devices, provides an efficient solution to microcomputer and many minicomputer-based product requirements.

CP1610 SYSTEM DIAGRAM



PROCESSOR SIGNALS

DATA BUS

D0-D15
Input/Output/High Impedance

Data 0-15: 16-bit bidirectional bus used to transfer data, addresses, and instructions between the microprocessor, memory, and peripheral devices.

PROCESSOR CONTROLS

$\overline{\text{STPST}}$
Input
SToP-STart: Edge-triggered by negative transition; used to control the running condition of the microprocessor.

HALT
Output
HALT: indicates that the microprocessor is in a stopped mode.

$\overline{\text{MSYNC}}$
Input
Master SYNC: Active low input synchronizes the microprocessor to the $\phi 1$, $\phi 2$ clocks during power-up initialization.

EBCA 0-3
Outputs
External Branch Condition Addresses 0-3: Address for one-of-16 external digital state tests via the BEXT (Branch on EXTernal) instruction.

EBCI
Input
External Branch Condition Input: Return signal from the one-of-16 selection made by EBCA 0-3.

BUS CONTROL SIGNALS

BDIR, BC1, BC2
Outputs
Bus DIRection, Bus Controls 1, 2: Bus control signals externally decoded to define the state of bus operations (see State Flow Diagram).

$\overline{\text{BUSRQ}}$
Input

$\overline{\text{BUSAK}}$
Output
BUS ReQuest, BUS AcKnowledge: BUSRQ* requests the microprocessor to relinquish control of the bus indefinitely. BUSAK* informs devices that the bus has been released.

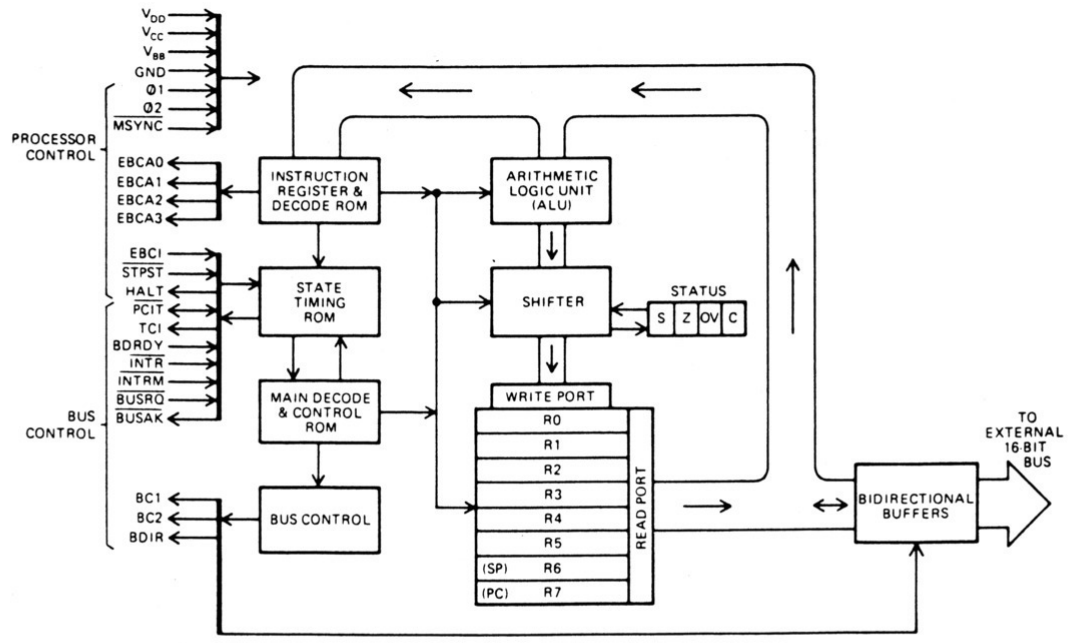
BDRDY
Input
Bus Data ReaDY: causes the microprocessor to "wait" and resynchronize to slow memory and peripheral devices.

$\overline{\text{INTR}}$, $\overline{\text{INTRM}}$
INTeRupt, INTeRupt Masked: request the microprocessor to service an interrupt upon completion of current instruction.

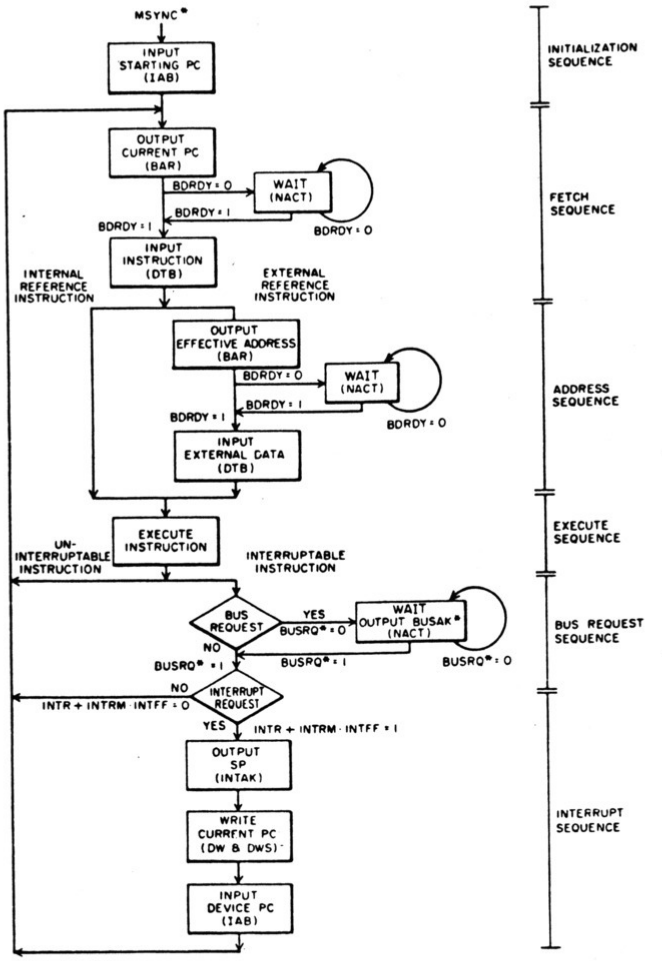
TCI
Output
Terminate Current Interrupt: pulse outputted by the microprocessor in response to the TCI instruction.

$\overline{\text{PCIT}}$
Input/output
Program Counter Inhibit/Trap: As an input, inhibits incrementation of the Program Counter during the instruction fetch sequence. As an output, generates a pulse during execution of a Software INterrupt (SIN) instruction.

CP1600 INTERNAL BLOCK DIAGRAM



SIMPLIFIED STATE FLOW DIAGRAM



BUS CONTROL SIGNALS

BDIR	BC1	BC2	Signal	Decoded Function
0	0	0	NACT	No ACTion, D0-D15 = high impedance
0	0	1	IAB	Interrupt Address to Bus, D0-D15 = Input
0	1	0	ADAR	Address Data to Address Register, D0-D15 = high impedance
0	1	1	DTB	Data to Bus, D0-D15 = Input
1	0	0	BAR	Bus to Address Register
1	0	1	DWS	Data Write Strobe
1	1	0	DW	Data Write
1	1	1	INTAK	INTerrupt AcKnowledge

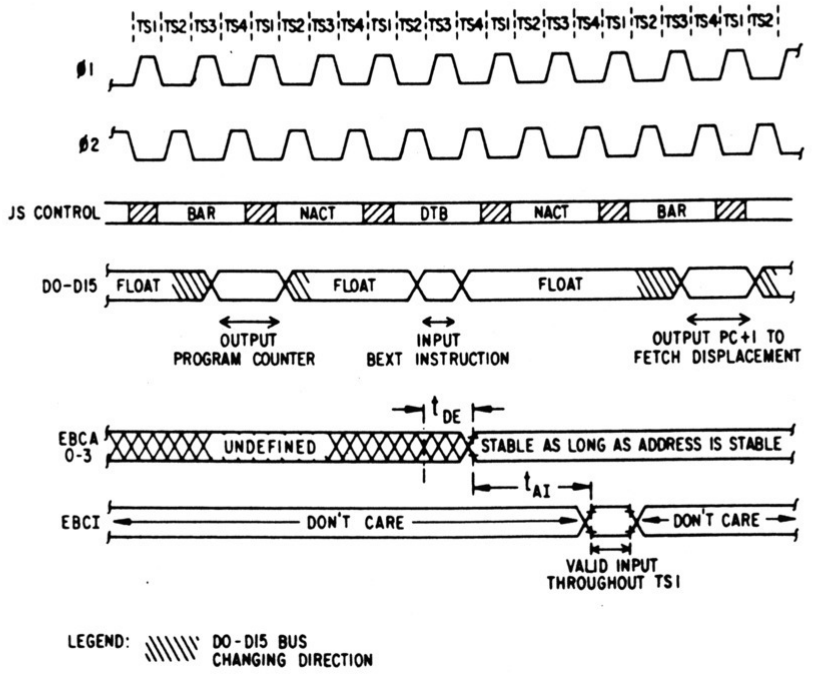
INSTRUCTION SET SUMMARY

		Mnemonics	Operation	Microcycles Dir.	Indr.	Imm.	Stack	Comments
External Reference Instructions	Arithmetic & Logic	ADD	ADD	10	8	8	11	
		SUB	SUBtract	10	8	8	11	
		CMP	CoMPare	10	8	8	11	Result not saved
		AND	logical AND	10	8	8	11	
		XOR	eXclusive OR	10	8	8	11	
	I/O	MVO	MoVe In	10	8	8	11	
		MVI	MoVe In	10	8	8	11	
Internal Register Instructions	Register to Register	ADDR	ADD contents of Registers	6				Add one cycle
		SUBR	SUBtract contents of Registers	6				if Register 6 or 7, except*.
		CMPR	CoMPare Registers by subtr.	6				Result not saved
		ANDR	logical AND Registers	6				
		XORR	eXclusive OR Registers	6				
		MOVR	MOVe Register	6				
	Single Register	CLRR	CLeaR Register	6				XORR with itself
		TSTR	TeST Register	6				
		JR	Jump to address in Register	7*				PC←(RRR)
		INCR	INCrement Register	6				
		DECR	DECrement Register	6				
		COMR	COMplement Register	6				One's Complement
		NEGR	NEGate Register	6				Two's Complement
		ADCR	ADd Carry Bit to Register	6				
		GSWD	Get Status WorD	6				
		NOP	No OPeration	6				Two Words
		SIN	Software INterrupt	6				Pulse to PCIT pin
		RSWD	Return Status WorD	6				
		PULR	PULl from stack to Register	11*				PULR=MVI @ R6
		PSHR	PuSH Register to stack	9*				PSHR=MVO @ R6
	Register Shift	SLL	Shift Logical Left	6				one or two position shift capability. Add two cycles for 2-position shift
		RLC	Rotate Left thru Carry	6				
		SLLC	Shift Logical Left thru Carry	6				
		SLR	Shift Logical Right	6				
		SAR	Shift Arithmetic Right	6				
		RRC	Rotate Right thru Carry	6				
		SARC	Shift Arithmetic Right thru Carry	6				
		SWAP	SWAP 8-bit bytes	6				2-position=SWAP twice
Control Instructions		HLT	HaLT	4				
		SDBD	Set Double Byte Data	4				Must precede external reference to double byte data
		EIS	Enable Interrupt System	4				
		DIS	Disable Interrupt System	4				
		TCI	Terminate Current Interrupt	4				Not Interruptible
		CLRC	CLeaR Carry to zero	4				
		SETC	SET Carry to one	4				
Jump Instructions		J	Jump	12				
		JE	Jump, Enable, interrupt	12				
		JD	Jump, Disable interrupt	12				
		JSR	Jump, Save Return	12				Return Address saved in R4, 5 or 6
		JSRE	Jump, Save Return & Enable	12				
		JSRD	Jump, Save Return & Disable Interrupt	12				
Conditional Branch Instructions		B	unconditional Branch	7				Displacement in PC+1
		BC, BLGE	Branch on Carry, C=1	7				PC←PC±Displacement
		BNC, BLLT	Branch on No Carry, C=0	7				Add 2 cycles if test condition
		BOV	Branch on OVerflow, OV=1	7				is true.
		BNOV	Branch on No OVerflow, OV=0	7				
		BPL	Branch on PLus, S=0	7				
		BMI	Branch on Minus, S=1	7				
		BZE, BEQ	Branch on ZEro or EQual	7				Z=1
		BNZE, BNEQ	Branch if Not ZEro or Not EQual	7				Z=0
		BLT	Branch if Less Than	7				S¥OV=1
		BGE	Branch if Greater than or Equal	7				S¥OV=0
		BLE	Branch if Less than or Equal	7				ZV(S¥OV)=1
		BGT	Branch if Greater Than	7				ZV(S¥OV)=0
		BUSC	Branch if Sign ≠ Carry	7				C¥S=1
		BESC	Branch if Sign = Carry	7				C¥S=0
		BEXT	Branch if External condition is True	7				4 LSB of Instruction are decoded to select 1 of 16 external conditions.

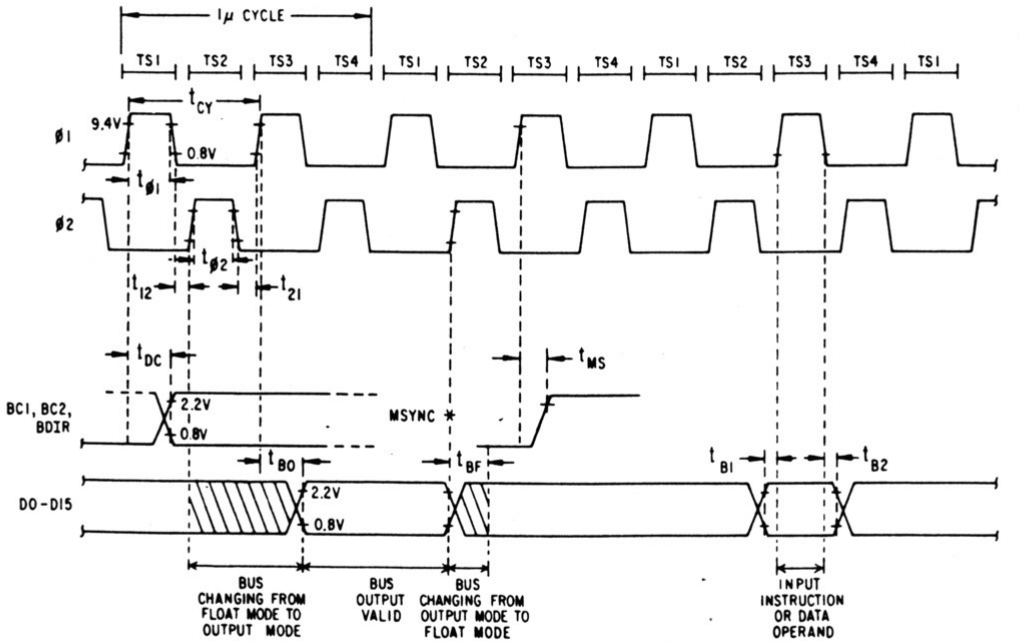
1 MICROCYCLE = 2 CLOCK CYCLES

TV GAMES

BUS TIMING DIAGRAM



TYPICAL INSTRUCTION SEQUENCE



BRANCH ON EXTERNAL CONDITION INSTRUCTION

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD}, V_{CC}, GND and all other input/output voltages with respect to V_{BB} . . . . . −0.3V to +18.0V
Storage Temperature . . . . . −55°C to +150°C
Operating Temperature . . . . . 0°C to +70°C

*Exceeding these ranges could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions: (unless otherwise noted)
V_{DD}=+11V±5%, 70mA(typ), 110mA(max.) V_{BB}= −3V±10%, 0.2mA(typ), 2mA(max.)
V_{CC}=+5V±5%, 12mA(typ), 25mA(max.) Operating Temperature (T_A)=0°C to +70°C

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Inputs						
High	V_{IHC}	10.0	–	V_{DD}	V	
Low	V_{ILC}	0	–	0.6	V	
Input current	—	—	—	15	mA	$V_{IHC} = V_{DD} - 1$
Logic Inputs						
Low	V_{IL}	0	–	0.65	V	
High (All Lines except BDRDY)	V_{IH}	2.4	–	V_{CC}	V	
High (Bus Data Ready Line See Note)	V_{IHB}	3.0	–	V_{CC}	V	
Logic Outputs						
High	V_{OH}	2.4	V_{CC}	—	V	$I_{OH} = 100\mu A$
Low (Data Bus Lines D0-D15)	V_{OL}	–	–	0.5	V	$I_{OL} = 1.6mA$
Low (Bus Control Lines, BC1,BC2,BDIR)	V_{OL}	–	–	0.45	V	$I_{OL} = 2.0mA$
Low (All Others)	V_{OL}	–	–	0.45	V	$I_{OL} = 1.6mA$
AC CHARACTERISTICS						
Clock Pulse Inputs, $\phi1$ or $\phi2$						
Pulse Width	$t\phi2$, $t\phi2$	250		–	ns	
Skew ($\phi1$, $\phi2$ delay)	t_{12}, t_{21}	0	–	–	ns	
Clock Period	t_{cy}	0.5	–	2.0	μs	
Rise & Fall Times	tr, tf	–	–	15	ns	
Master SYNC:						
Delay from ϕ	tms	–	–	30	ns	
D0-D15 Bus Signals						
Output delay from $\phi1$ (float to output)	t_{BO}	–	–	200	ns	1 TTL Load & 25 pF
Output delay from $\phi2$ (output to float)	t_{BF}	–	50	–	ns	
Input setup time before $\phi1$	t_{B1}	0	–	–	ns	
Input hold time after $\phi1$	t_{B2}	10	–	–	ns	
Bus Control Signals . BC1,BC2,BDIR						
Output delay from $\phi1$	t_{DC}	–	–	200	ns	
BUSAK Output delay from $\phi1$	t_{BU}	–	150	–	ns	
TCI Output delay from $\phi1$	t_{TO}	–	200	–	ns	
TCI Pulse Width	t_{TW}	-	300	–	ns	
EBCA output delay from BEXT input	t_{DE}	–	–	150	ns	
EBCA wait time for EBCI input	t_{AI}	–	–	400	ns	
CAPACITANCE						TA = +25°C; V_{DD} = +12V; V_{CC} = +5V; V_{BB} = −3V; $t\phi1$ t $\phi2$ = 120ns
$\phi1$, $\phi2$ Clock Input capacitance	C$\phi1$, C$\phi2$	—	20	30	pF	
Input Capacitance						
D0-D15	CIN	—	6	12	pF	
All Other	—	—	5	10	pF	
Output Capacitance						
D0 -D15 in high impedance state	C_D	—	8	15	pF	

**Typical values are at +25°C and nominal voltages.

NOTE: The Bus Data ReaDY(BDRDY) line is sampled during time period TSI after a BAR or ADAR bus control signal. BDRDY must go low requesting a wait state 50 ns before the end of TS1 and remain low for 50 ns minimum. BDRDY may go high asynchronously. In response to BDRDY, the CPU will extend bus cycles by adding additional microcycles up to a maximum of 40 μsec duration.

20480 Bit Static Read Only Memories

FEATURES

- 2048 × 10 bit ROM organization
- Address and data on single 16 bit tristate bus
- 5 bit programmable chip select
- Output address latches and control signals generated for controlling up to 1K of external RAM (RO-3-9501) or up to 65K of external RAM (RO-3-9502).
- Internal address status and data bits latched
- 300 ns typical data access time
- 1.8μs complete cycle time
- TTL compatible I/O
- Single +5 Volt power supply
- Ideal for microprocessors with multiplexed I/O bus for address and data.
- Totally automated custom programming
- 16 bit programmable initialization and interrupt response addresses output to I/O bus

DESCRIPTION: RO-3-9501

The RO-3-9501 is a unique 20,480 bit ROM employing a single 16 bit address and data tristate buss. The RO-3-9501 increases the power of single buss microprocessors or microcontrollers by providing separate latched address and control lines for static RAM chips. The RO-3-9501 internally decodes ROM and external RAM control codes. ROM addressing is via an 11-bit word address and a 5-bit chip select code. Ten bit data is outputted on the lower 10 bits of the I/O buss. In addition there are two programmable 16-bit interrupt response codes, one for the first interrupt after master clear and one for all other interrupts. These codes are output to the I/O bus in response to control codes, which do not require a chip select code. The RO-3-9501 contains a 10 bit latch and address output port; the 10-bit address appearing at this port may be used to control an external RAM. The address is latched by a control code on the three mode control lines, and the RAM enable signal which consists of all zeros on data bits 11 through 15. The stored address is copied from bits 0 through 9 on the data buss.

The RO-3-9501 has two programmable features, in addition to the 2048 word by 10-bit ROM. A five bit chip select code decodes data bits 11 through 15 in order to generate the internal chip enable signal. Second, the two 16-bit interrupt response codes are programmable.

DESCRIPTION: RO-3-9502

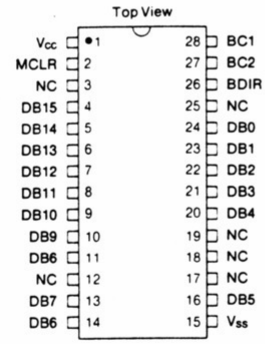
The RO-3-9502 has all the features of the RO-3-9501 described above except that it has a full 16-bit latch and address port for external RAM.

DESCRIPTION: RO-3-9500

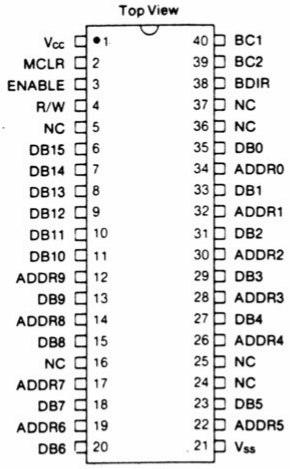
The RO-3-9500 does not provide address facilities for external RAM allowing for its packaging in a 28 lead DIP.

PIN CONFIGURATIONS

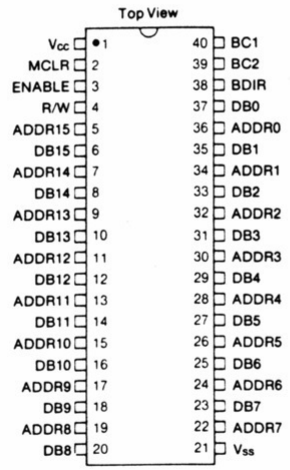
28 LEAD DUAL IN LINE
RO-3-9500



40 LEAD DUAL IN LINE
RO-3-9501



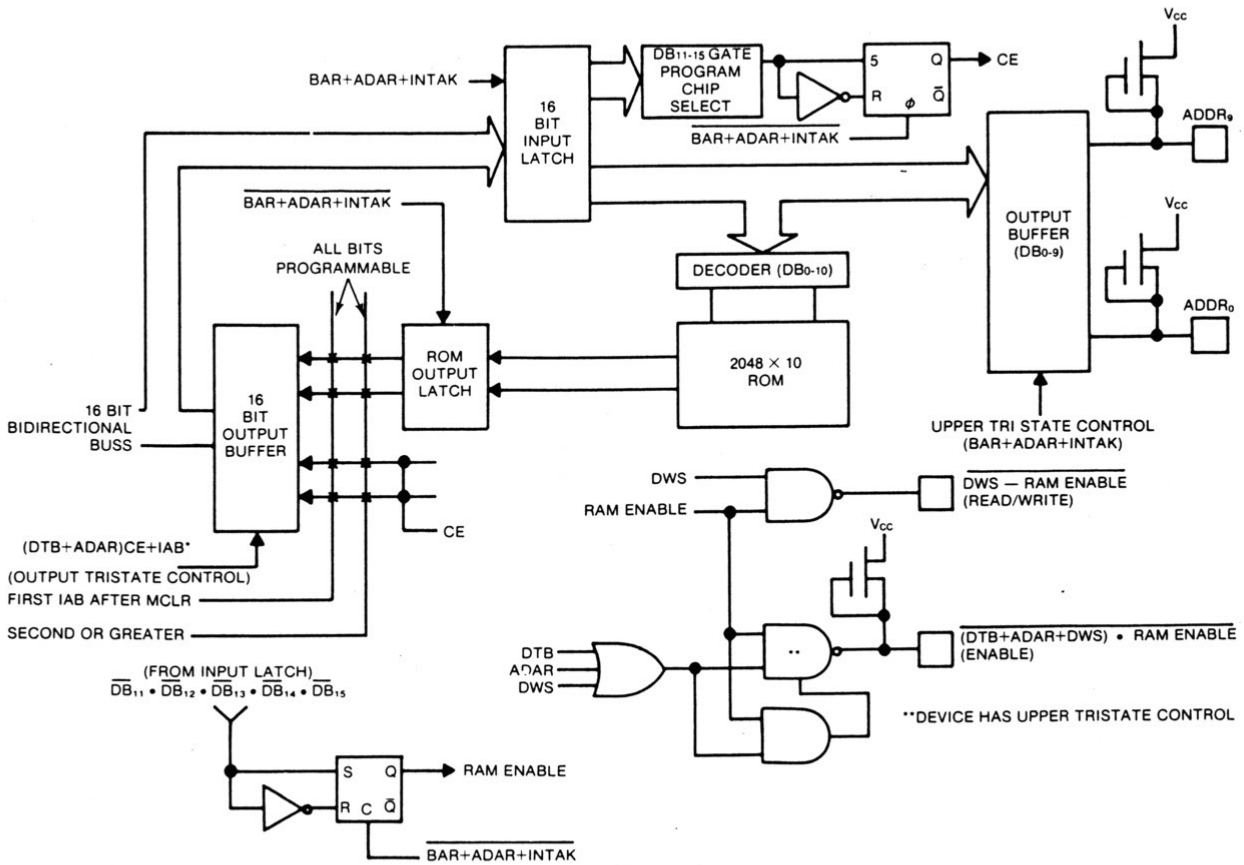
RO-3-9502



PIN FUNCTIONS

Enable (RO-3-9501/02)	An ouput pin to select external RAM (low = true)
R/W (RO-3-9501/02)	An output pin for read/write control of external RAM, a positive pulse controls the write cycle.
ADDR0-9 (RO-3-9501) ADDR0-15 (RO-3-9502)	Output address lines to external RAMs.
DB0-DB15	Bidirectional, tristate data and address buss, high output impedance for NACT control code.
BC1, BC2 BDIR	Buss control 1 and 2, and buss direction control signals determine chip mode control
V_{CC}	+5 volts
V_{SS}	Ground
MCLR	Master clear, sets all outputs to high impedance state when low.

BLOCK DIAGRAM: RO-3-9501



NOTES:

1. Input data and internal chip enable latched by control codes = BAR + ADAR + INTAK
2. Internal chip enable signal cleared by = BAR + ADAR + INTAR
3. Internal RAM enable signal flip flop set by PB11-15 all zeros, cleared by = BAR + ADAR + INTAK
4. RAM enable plus DWS creates low on Read/Write line.
5. RAM enable plus DTB, ADAR or DWS creates enable output signal.
6. DTB or ADAR plus internal chip enable puts output ROM data to tristate buss.
7. Maximum skew time between control code transitions is 40 nsec to avoid false states.
8. Enable R/W and ADDRO — 9 lines normally high impedance outputs. When circuits are enabled, active pull up transistors turned on to allow wired or connection to other chips. RAM control signals and output addresses revert to high impedance state in 2 and 0 - 3μsec respectively. After master clear, chip enable and RAM enable flip-flops turned off and all outputs in high impedance states.

OPERATING MODES

The RO-3-9501 is designed to enhance the system operation of 16-bit Microprocessors that use a single multiplexed buss for data and memory addresses, such as the GI CP1600, the Intel 8085 and the Fairchild 9440. The state diagram shows recommended sequences for initialization, programstorage with RAM addressing, and interrupt handling.

The three mode control lines BC1, BC2 and BDIR create 8 functions. As shown in figure one, these functions are chosen to simplify program and data storage in the ROM. Functionally the RO-3-9501 performs the following functions in a microprocessor system:

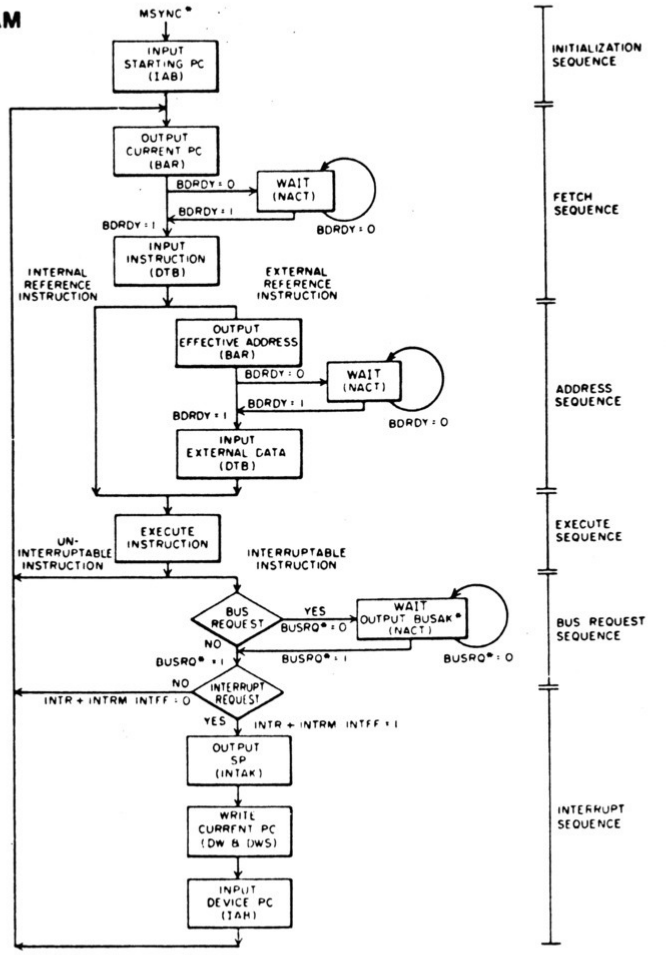
A. When the CPU generates a 5 chip select and seven bits of ROM address, the RO-3-9501 generates a 10-bit response from the 2048 × 10 bit ROM.

B. The ROM output data can be used to create a ten-bit immediate or indexed RAM address, which is then stored in the RO-3-9501 ten output latches and the RAM control lines. In addition the RAM enable and R/W control lines are generated by inernal logic.

C. In response to initial clear and the first interrupt, the RO-3-9501 can be programmed to place a 16-bit trap address on the I/O buss for restarting a chosen program sequence. The RO-3-9501 can additionally be programmed to generate a different 16-bit trap address in response to subsequent IAB's.

For the IAB (Interrupt Address to Buss) commands to work properly, an address must first be loaded into the chip to disable the internally latched chip enable code.

SIMPLIFIED STATE FLOW DIAGRAM



BUS CONTROL SIGNALS

BDIR	BC1	BC2	Signal	Decoded Function
0	0	0	NACT	No ACTion, D0-D15 = high impedance
0	0	1	IAB	Interrupt Address to Bus, D0-D15 = Input
0	1	0	ADAR	Address Data to Address Register, D0-D15 = high impedance
0	1	1	DTB	Data to Bus, D0-D15 = Input
1	0	0	BAR	Bus to Address Register
1	0	1	DWS	Data Write Strobe
1	1	0	DW	Data Write
1	1	1	INTAK	INTerrupt AcKnowledge

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD} and all other input/output voltages with respect to GND .....−0.3V to +18V
Storage Temperature ..... −55°C to 150°C
Operating Temperature ..... 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

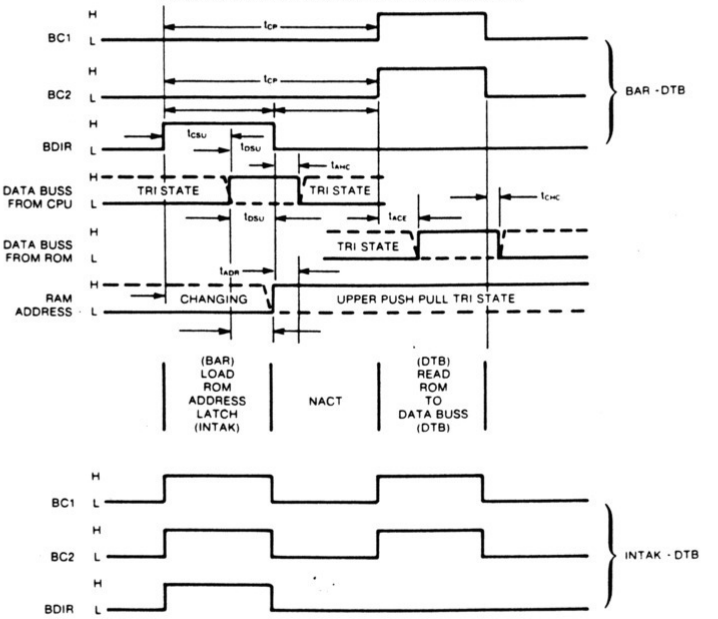
Standard Conditions (unless otherwise noted)

All voltages referenced to GND
V_{DD} = +12V ±5%
Operating Temperature (T_A) = 0°C to +75°C

Standard Conditions (V_{CC} = 5±10%; t = 0°, 70°C)

Characteristic	Symbol	Min.	Typ.*	Max.	Units	Conditions
DC CHARACTERISTICS						
Logic '0' Input	V_{IL}	0	—	0.6	V	
Logic 'I' Input	V_{IH}	1.4	—	V_{CC}	V	
Logic '0' Output	V_{OL}	0	—	0.4	V	I_{sink} = 1mA
Logic 'I' Output	V_{OH}	2.2	—	V_{CC}	V	I_{source} = 100μA
Input leakage	I_L	—	—	10	μA	
Power Supply Current	I_{CC}	60	—	70	mA	V_{CC} = 5.0V
AC CHARACTERISTICS						
ROM Data Access	t_{ACC}	250	—	350	ns	Fig. 1,5
ROM Data Hold	t_{AHC}	50	—	300	ns	Fig. 1,5
RAM Address Setup	t_{ADR}	150	—	250	ns	Fig. 1, 2, 3, 4
Control Setup	t_{CSU}	500	—	—	ns	Fig. 1
Address Setup	t_{ASU}	300	—	—	ns	Fig. 1
Control Hold Time	t_{OHC}	50	—	—	ns	Fig. 1
No Action Time	t_{NACT}	0	—	2000	ns	Fig. 1
Control Period	t_C	800	—	—	ns	Fig. 1, 2, 3, 4, 5
Code Time	t_{CP}	1600	—	2800	ns	Fig. 1, 2, 3, 4
No Action Time	t_{NACT}	500	—	2000	ns	Fig. 2, 3, 5
Data Setup	t_{DSU}	—	—	300	ns	Fig. 1, 2
RAM Address Hold	t_{AHR}	300	—	2000	ns	Fig. 2, 3, 4
RAM Access Time	t_{ACR}	150	—	300	ns	Fig. 2, 3
Master Clear	t_{MC}	100	—	10,000	ns	Fig. 5

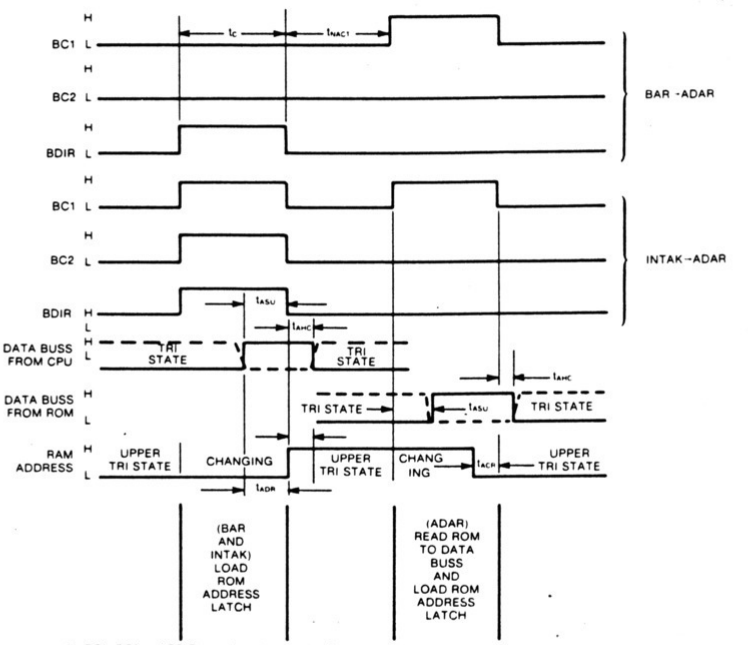
20K ROM
BAR/INTAK INSTRUCTION FOLLOWED BY DTB INSTRUCTION



* Minimum hold time after DTB before going tristate. Maximum time to tristate = 300ns (all time in nSec)
** BC1, BC2 and BDIR are return to zero signals
*** Upper tristate means that the upper push pull output device is disabled and an internal load resistor will hold the output positive
**** Proper CE address must be latched to allow ROM output to function during DTB
***** Since chip is assumed to be selected R/W and RAM enable remain in the high state

Fig. 1

20K ROM
BAR/INTAK INSTRUCTION FOLLOWED BY ADAR INSTRUCTION



** BC1, BC2 and BDIR are return to zero signals
*** Proper CE address must be latched to allow ROM output to function during DTB
**** Since chip is assumed to be selected R/W and RAM enable remain in the high state

Fig. 2

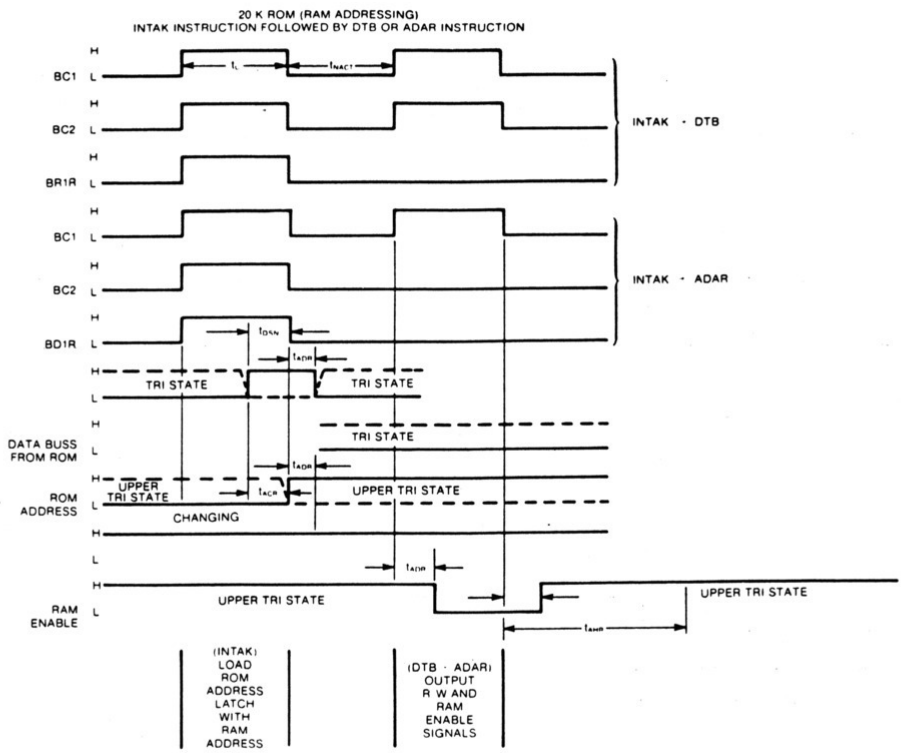
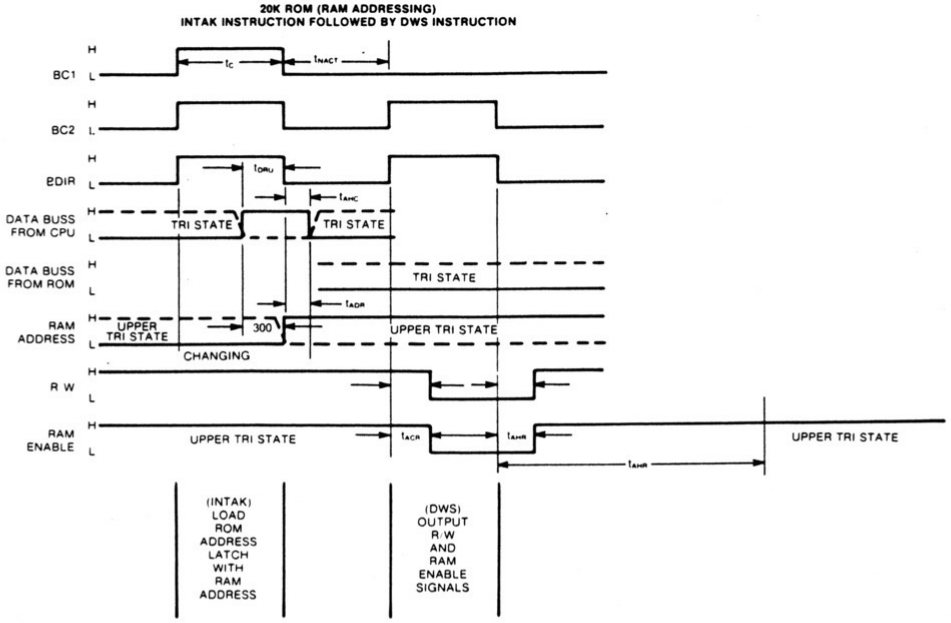


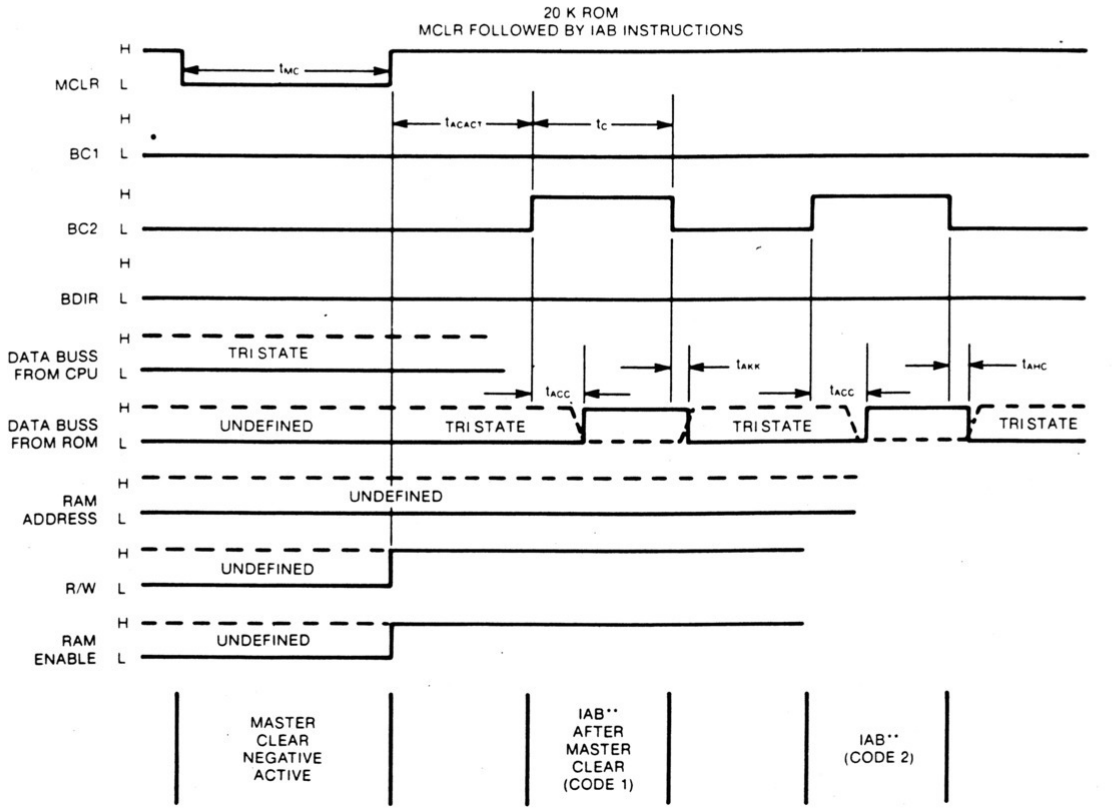
Fig. 3



* Maximum time to upper tri state condition
** RAM address has DB_{11} thru DB_{15} = Logic '0'
*** BAR or ADAR can be used instead of INTAK to load RAM address. If ADAR is used remember RAM address will be provided from ROM output to data buss if chip previously enabled
(All time in nSec)

Fig. 4

TV GAMES



* Minimum hold time after IAB before going tri state. Maximum time to tri state = 300 ns
** The first IAB after master clear will present a 16 bit programmable code to the data buss. Subsequent IAB instructions will output a second code that is gate programmable on ROM chip.
(All time in nsec)

Fig. 5

2112A

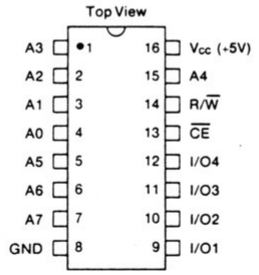
1024 Bit Static RAM

FEATURES

- 256 x 4 organization.
- 350 ns access time.
- TTL compatible.
- Fully static-no clocks required.
- Single +5V supply.

This circuit is not manufactured by General Instrument Microelectronics. The information is provided for reference only.

PIN CONFIGURATION
16 LEAD DUAL IN LINE



2114

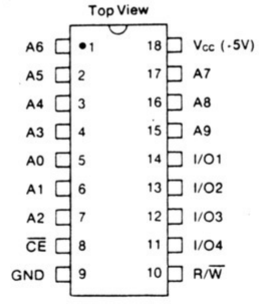
4096 Bit Static RAM

FEATURES

- 1024 x 4 organization.
- 450 ns access time.
- TTL compatible.
- Fully static-no clocks required.
- Single +5V supply.

This circuit is not manufactured by General Instrument Microelectronics. The information is provided for reference only.

PIN CONFIGURATION
18 LEAD DUAL IN LINE



AY-3-8910

PRELIMINARY INFORMATION

Programmable Sound Generator

FEATURES

- Full software control of sound generation.
- Interfaces to most 8-bit and 16-bit microprocessors.
- Three independently programmed analog outputs.
- Two 8-bit I/O ports for general use.
- Single +5 Volt supply.

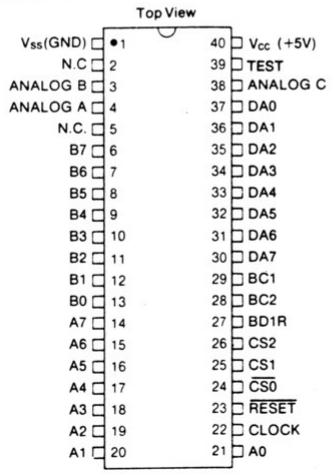
DESCRIPTION

The AY-3-8910 is a Large Scale Integrated Circuit that can produce a wide variety of complex sounds under software control. It is easily interfaced to most 8 and 16-bit microprocessors; however, it is optimally designed to directly connect to the CP1600 series of microprocessors. The flexibility of the AY-3-8910 makes it useful in applications such as music synthesis, sound effects, audible alarms, and FSK modems. In addition, once interfaced, the AY-3-8910 provides the microprocessor with two parallel 8-bit bi-directional data ports that are TTL compatible. The analog sound outputs can each provide 4 bits of logarithmic D/A conversion.

The AY-3-8910 is manufactured in the N-Channel Ion Implant process. Operation requires a single 5V supply, a 2 MHz TTL clock and a microprocessor controller such as the 1600 series.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



HARDWARE ARCHITECTURE

The AY-3-8910 is designed to interface directly to the GI CP1600/1610 microprocessor as well as all one-chip microcomputers with 11 or more programmable I/O lines, such as:

GI PIC Series
TI TMS 1000 Series
Intel 8000 Series

The 11 I/O lines used by the one-chip processors to interface to the AY-3-8910 are returned as 16 programmable TTL compatible I/O lines on the AY-3-8910.

Commands are issued to the AY-3-8910 thru the use of memory operations at the appropriate address. Sixteen registers within the AY-3-8910 control the analog outputs and parallel I/O ports. Each of these registers correspond to a memory location displaced from the AY-3-8910 Base Address by the register number.

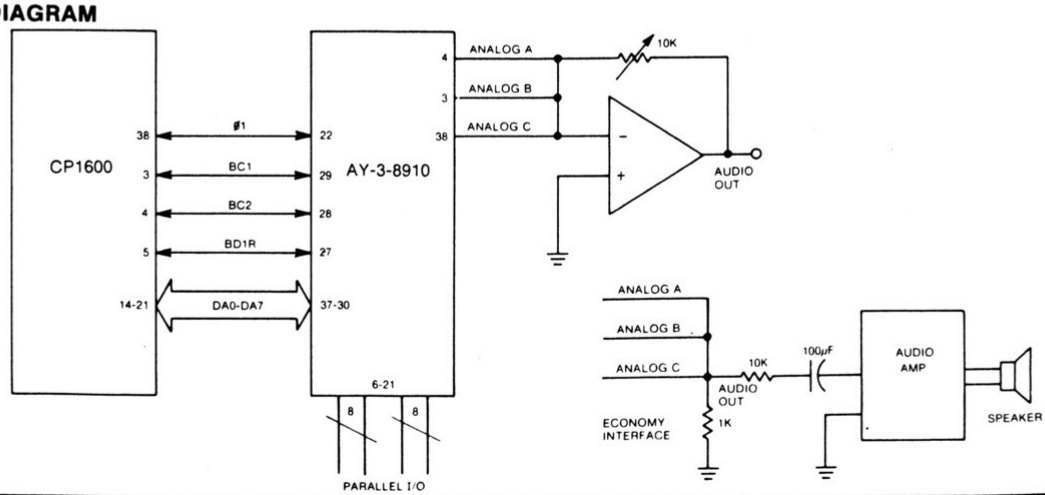
SOFTWARE ARCHITECTURE

Communication between the controller and the AY-3-8910 is based on the concept of memory mapped I/O. With a controller such as the CP 1600 the AY-3-8910 looks like a block of memory. Parallel input and output, as well as programming the three analog outputs for complex sounds is accomplished by performing memory operations on the appropriate memory location.

The AY-3-8910 memory block is organized as 16 consecutive memory locations starting at the base address which is decoded by the chip select lines. (CS0-CS2).

All of the registers are readable so that the controller can determine the present state of the AY-3-8910.

SYSTEM DIAGRAM



PIN FUNCTIONS

Signal	Functional Description
Clock (input)	2MHz Clock—this input is a reference for timing within the AY-3-8910.
DA0-DA7 (input/output)	Data/Address Bus Bits 0-7 — this 8-bit bus passes all data and address information between the AY-3-8910 and the controller.
CS0-CS2 (input)	Chip Select Lines—a three bit code on these lines selects the AY-3-8910 for sound programming or parallel input/output.
BC1, BC2, BD1R (input)	Bus Control Signals (ref. Fig. 7) — generated by the controller these lines decoded within the AY-3-8910 to control all bus operations.
$\overline{\text{RESET}}$ (input)	Reset — clears the AY-3-8910 on power up.
IOA0-IOA7 (input/output) IOB0-IOB7 (input/output)	Parallel Input/Output Ports—each of these ports provide 8 bits of parallel data for use by the external world. These ports are each programmable for either input or output and are TTL compatible.
ANALOG A, B, C (outputs)	Analog Outputs — each of these outputs are independently programmable to produce complex sounds.
TEST	For GI test-normally not connected.

16 REGISTER MEMORY MAP FOR AY-3-8910

REGISTER		B7	B6	B5	B4	B3	B2	B1	B0
R0	Channel A Period	8-BIT Fine Tune							
R1	Channel B Period	8-BIT Fine Tune							
R2	Channel C Period	8-BIT Fine Tune							
R3	Envelope Period	8-BIT Fine Tune							
R4	Channel A Period	4-BIT Course Tune							
R5	Channel B Period	4-BIT Course Tune							
R6	Channel C Period	4-BIT Course Tune							
R7	Envelope Period	8-BIT Course Tune							
R10	Enable	IOB OUT	IOA OUT	Noise $\overline{C}$	Noise $\overline{B}$	Noise $\overline{A}$	Tone $\overline{C}$	Tone $\overline{B}$	Tone $\overline{A}$
R11	Noise Gen. Clock			5-BIT Period Control					
R12	Envelope Control					CON.	ATT.	ALT.	HOLD
R13	Channel A			C1	C0	D3	D2	D1	D0
R14	Channel B								
R15	Channel C								
R16	IOA	8-BIT PARALLEL I/O on Port A							
R17	IOB	8-BIT PARALLEL I/O on Port B							

NOTE: For Registers 13, 14, 15

C1	C0	Expected Output (LOG AMPLITUDE)				
1	1	E3	E2	E1	E0	(Ref. Figs. 1 and 2)
1	0	0	E3	E2	E1	
0	1	0	0	E3	E2	
0	0	D3	D2	D1	D0	

WHERE: E3 E2 E1 E0 Come From the Envelope Generator
D3 D2 D1 D0 Are the Lower 4 BITS of R13, R14, R15
C1 C0 Are the Upper 2 BITS of R13, R14, R15

Channel A, B, C Is Shut off by Zeroing R13, R14, R15 Respectively.

REGISTER # (octal)	ADDRESS (octal)	BITS	FUNCTION NAME	DESCRIPTION
R0	Base	8	f0	Fine tunes frequency on channel A. 8 bits are proportional to period.
R1	Base + 1	8	f1	Similar to f0 but channel B.
R2	Base + 2	8	f2	Similar to f0 but channel C.
R3	Base + 3	8	fE	Fine tunes envelope period.
R4	Base + 4	4	P0	Coarse tunes channel A (high four bits).
R5	Base + 5	4	P1	Coarse tunes channel B (high four bits).
R6	Base + 6	4	P2	Coarse tunes channel C (high four bits).
R7	Base + 7	8	PE	Coarse tunes the envelope period.
R10	Base + 10	8	$\overline{\text{Enable}}$	Each bit controls a unique function (active low): Bit 0: Tone on channel A. Bit 1: Tone on channel B. Bit 2: Tone on channel C. Bit 3: Noise on channel A. Bit 4: Noise on channel B. Bit 5: Noise on channel C. Bit 6: IOA, 0 for input, 1 for ouput. Bit 7: IOB, 0 for input, 1 for output.
R11	Base + 11	5	N Clock	Varies the frequency of the clock for the noise generator.
R12	Base + 12	4	Envelope Control	Each bit controls a function in the envelope generator: Bit 0: Hold. Holds the last count of the specified envelope. Bit 1: Alternate. The amplitude of the envelope generator cycles up and then down. Bit 2: Attack. When high, the envelope will attack. When low, the envelope will decay. Bit 3: Continue. When high, the analog output will not shut off after one cycle. When low, the analog output shuts off after one cycle.
R13	Base + 13	6	Envelope A	Each of these registers controls its respective envelope in the following way (also refer to Note in memory map above): Bit D0 - Bit D3 - These bits directly control the amplitude of each analog output when bits 4 and 5 are low.
R14	Base + 14	6	Envelope B	
R15	Base + 15	6	Envelope C	
R16	Base + 16	8	IOA	With the control bits of R10 set for the output mode, data can be written to these ports from the CPU, and latched. With the control bits set for input, data can be read into the CPU. Each port is independently programmable.
R17	Base + 17	8	IOB	

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Storage Temperature ..... −55°C to +150°C
Operating Temperature ..... 0°C to +40°C
V_{CC} and all other input and output voltages with respect to V_{SS} ..... −0.3°C to +8.0V

*Exceeding these ratings could cause permanent damage to this device. Functional operation at these conditions is not implied—operating conditions are specified below.

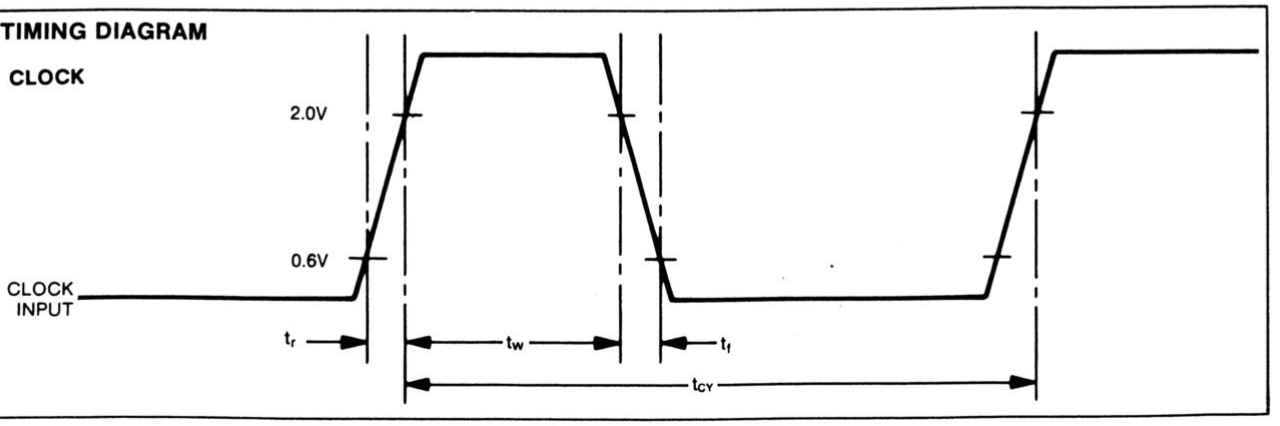
STANDARD CONDITIONS (unless otherwise noted)

V_{CC} = +5V ±5%
V_{SS} = GND
Operating Temperature: 0°C to 70°C

Characteristic	Symbol	Min.	Typ.**	Max.	Units	Conditions
DC CHARACTERISTICS						
Power Supply Current	I_{CC}	–	45	75	mA	
Logic Inputs (all inputs)						
Low	V_{IL}	0	–	.6	V	
High	V_{IH}	2.4	–	V_{CC}	V	
Logic Outputs (all outputs except Analog outputs)						
Low	V_{OL}	0	–	.55	V	I_{OL} = 1.6 mA
High	V_{OH}	2.4	–	V_{CC}	V	I_{OH} = 100 μA
Leakage (A0-A7, B0-B7, DA0-DA7)	I_{OH}	–	TBD	–	μA	
Logic Outputs (Analog Outputs)						
Low	V_{OL}	–	TBD	–	V	
High	V_{OH}	–	TBD	–	V	
AC CHARACTERISTICS						
Clock Input						
Period	t_{CY}	500	–	750	ns	
Rise time	t_r	–	–	50	ns	
Fall time	t_f	–	–	50	ns	
Pulse width	t_W	–	–	150	ns	
DA0-7 Bus Signals						
Output delay from bus control (tristate to output)	t_{DA}	–	–	250	ns	
Output delay from bus control (output to tristate)	t_{OH}	20	–	100	ns	
Input hold time after BDIR	t_{IH}	100	–	–	ns	
Input Pulse width	t_{IW}	300	–	–	ns	
Input Setup time	t_{IA}	–	TBD	750	ns	
Data Input Setup time	t_{DI}	–	–	750	ns	
Data Input Hold time	t_{DH}	100	–	–	ns	
Data Write Pulse	t_{DW}	1.5	–	–	μs	
Analog Outputs	–	–	TBD	–	–	

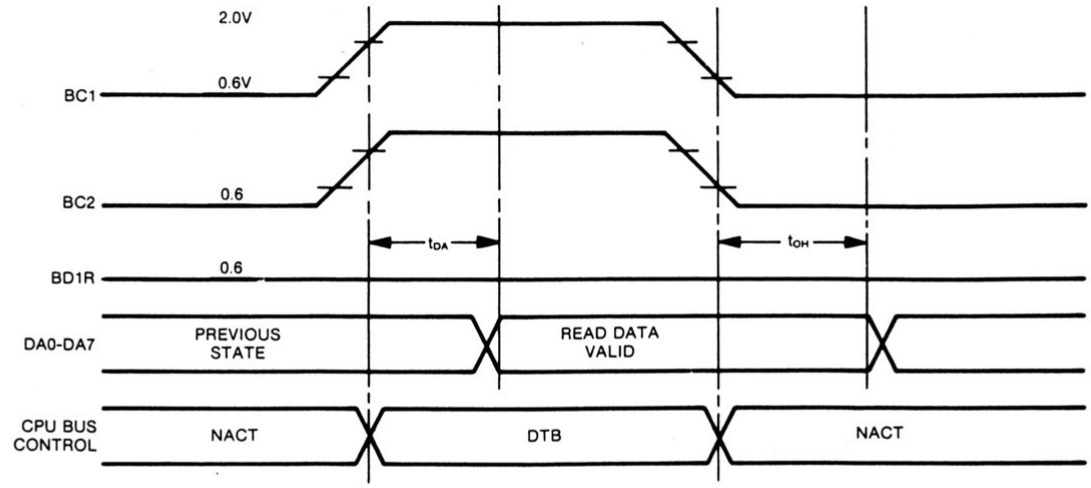
**Typical values are at 25°C and nominal voltages.

TIMING DIAGRAM

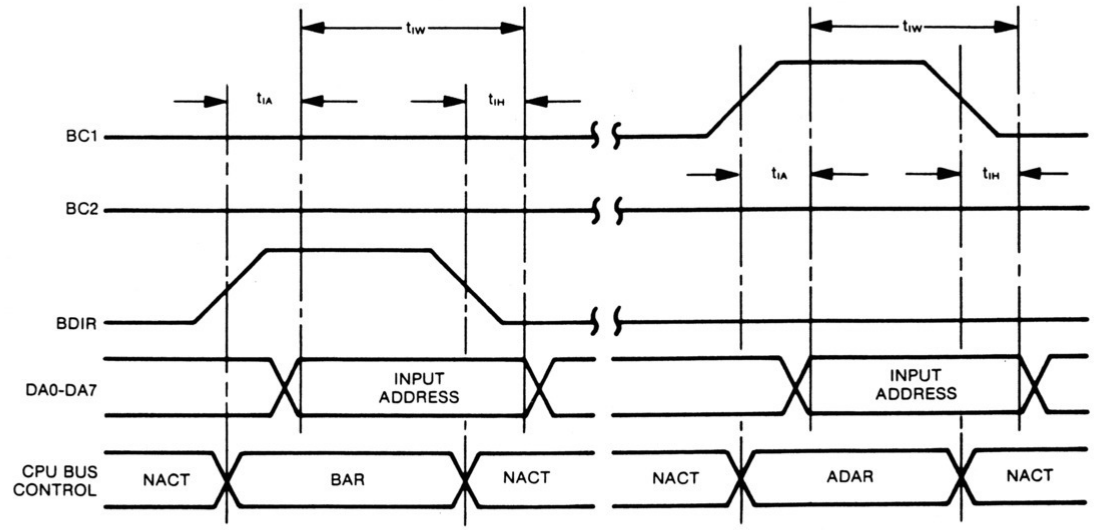


TIMING DIAGRAMS

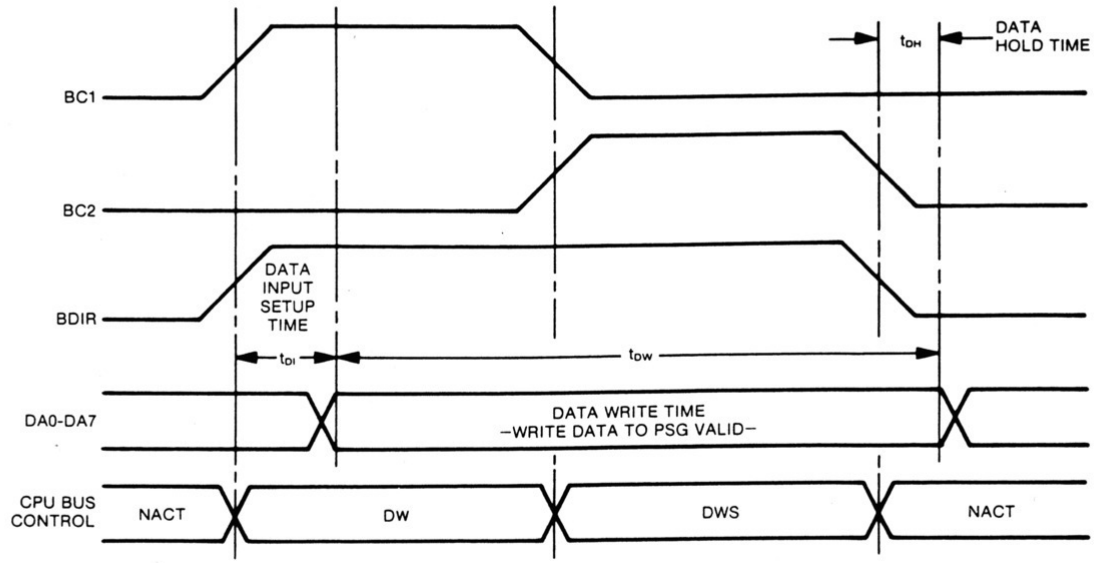
READ BUS TIMING



ADDRESS BUS TIMING



DATA WRITE TIMING



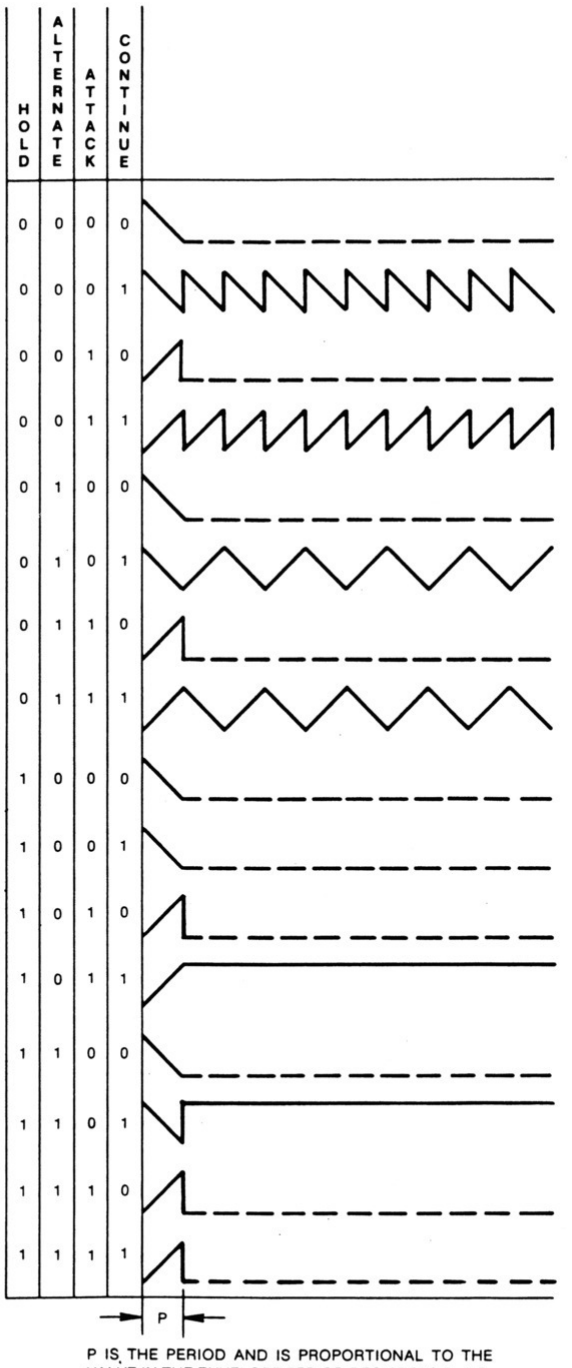


Fig.1 SAMPLE OF SOME WAVEFORMS AVAILABLE FROM THE ENVELOPE GENERATOR.

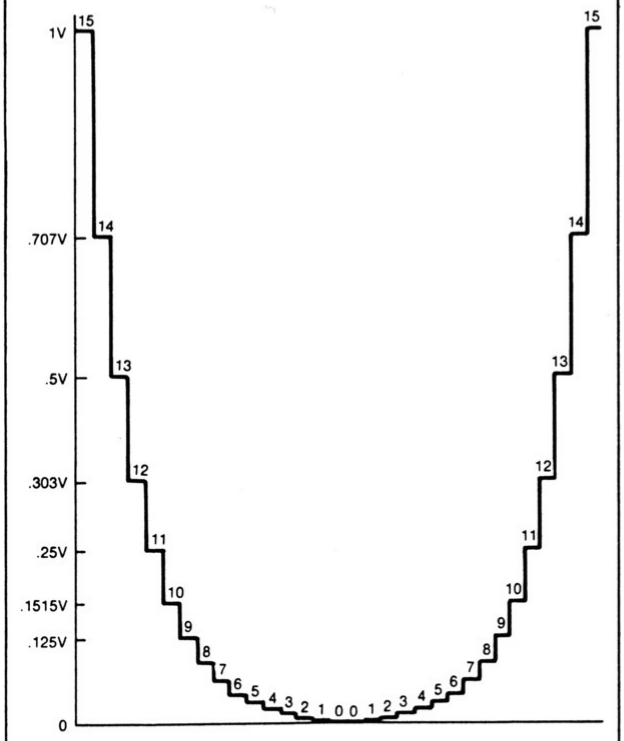


Fig.2 IDEAL LOGARITHMIC OUTPUT OF D/A CONVERTER WITH NO MUTING

TYPICAL OUTPUT WAVEFORMS

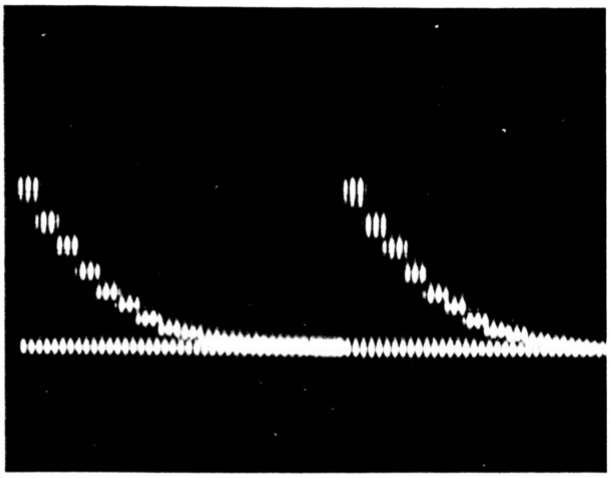


Fig. 3 $R0_8 = 14_8$, $R3_8 = 37_8$, $R12_8 = 10_8$, $R13_8 = 77_8$, ALL OTHER REGISTERS = 0.

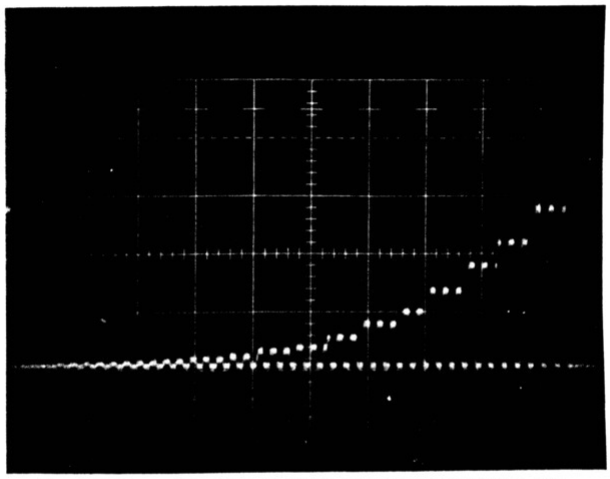


Fig. 4 $R12_8 = 14_8$, ALL OTHER REGISTERS SAME AS Fig. 3.

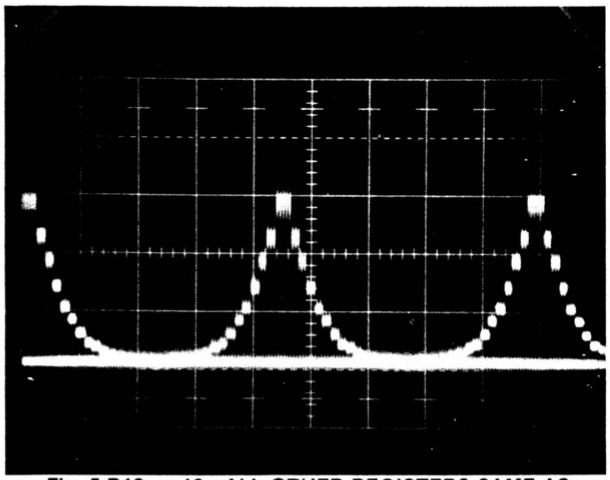


Fig. 5 $R12_8 = 12_8$, ALL OTHER REGISTERS SAME AS Fig. 3.

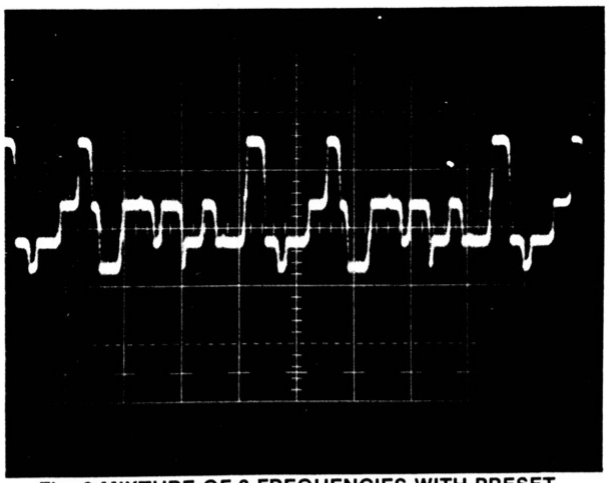


Fig. 6 MIXTURE OF 3 FREQUENCIES WITH PRESET AMPLITUDES.

BDIR	BC1	BC2	Signal	Decoded Function
0	0	0	NACT	No ACTion.
0	0	1	IAB	Interrupt Address to Bus.
0	1	0	ADAR	Address Data to Address Register.
0	1	1	DTB	Data to Bus.
1	0	0	BAR	Bus to Address Register
1	0	1	DWS	Data Write Strobe
1	1	0	DW	Data Write
1	1	1	INTAK	INTerrupt AcKnowledge

Fig. 7 BUS CONTROL SIGNALS

GIMINI Deluxe "8900" Programmable Game System

FEATURES

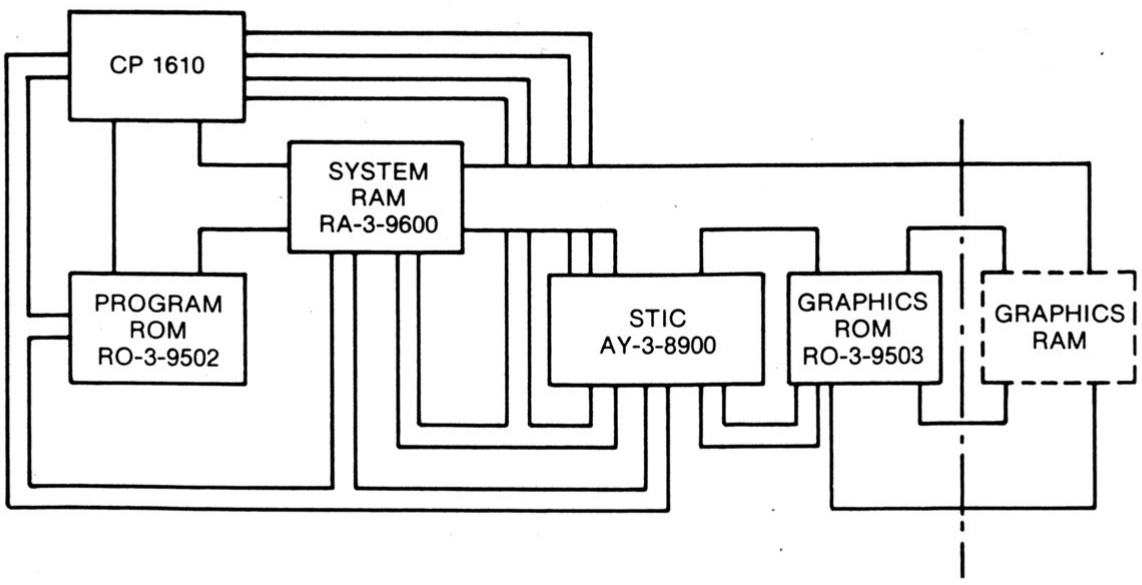
- Infinite game selection
- Lowest cost expandable system
- Uses programmable 20K ROMs
- Eight color selectable, coordinate addressable game objects on a grid of 160H by 96V.
- Resident library of 256 complex game objects, including full 64 character alpha numerics
- Shape library extenable by a further 256 objects using graphics RAM.
- Full multicolor background capability
- Sixteen selectable color tones
- Program controllable moving background
- Two hundred and forty independently programmable background locations

DESCRIPTION

The GIMINI 8900 system is based on two processors; one computes the game action against the stored program rules; and the second interprets a condensed memory area and uses this to generate the T.V. raster display. The second processor fetches moving and background pictures from the graphic picture storage and presents the data as a video output.

The set consists of five General Instrument supplied N-Channel circuits. The AY-3-8900 Standard Television Interface Circuit (STIC); the CP1610 GIMINI Microprocessor; an RO-3-9502 20K program ROM; a similar RO-3-9503 graphics picture ROM and an RA-3-9600 RAM. To complete the system the user supplies clocking and modulation circuitry plus any other peripheral control requirements.

8900 SYSTEM DIAGRAM



8900 SYSTEM COMPONENTS

DESCRIPTION	PART NUMBER	GAME FUNCTION	PACKAGE	FEATURES
BASIC COMPONENTS: A complete microprocessor programmable game with only 5 LSI chips, the GIMINI Deluxe "8900" offers the capability for maximum game flexibility with detailed graphics definition and manipulation.	CP1610	MICROPROCESSOR	40 DIP	A full 16-bit microprocessor for processing all game data.
	AY-3-8900	TV INTERFACE	40 DIP	Processes graphics data and generates all video signals.
	AY-3-8900-1			
	RO-3-9502	PROGRAM ROM	40 DIP	A 2048 x 10 ROM which contains the executive program.
	RO-3-9503	GRAPHICS ROM	40 DIP	A 2048 x 8 ROM which stores 256 - 8 x 8 graphics characters.
	RA-3-9600	SYSTEM RAM	40 DIP	Contains a 352 x 16 memory plus a 20 word "current line" buffer.
OPTIONAL COMPONENTS: The basic "8900" system can easily be expanded to include additional games plus software-controlled graphics interaction, complex sound generation, and supplementary peripherals.	RO-3-9500	CARTRIDGE ROM	28 DIP	A 2048 x 10 ROM which contains additional game programs.
	2112A/2114	PROGRAM/ GRAPHICS RAM	16/18 DIP	Customer-supplied 256 x 4 or 1K x 4 RAMs to increase system capabilities.
	AY-3-8910	SOUND GENERATOR	40 DIP	Provides programmed generation of complex sound effects.
	AY-3-8915	COLOR PROCESSOR	16 DIP	Generates a single composite color signal from AY-3-8900-1 digital input.
	AY-3-8920	TAPE CASSETTE INTERFACE	40 DIP	Interfaces system to standard audio cassette decks.
	IOB 1680	INPUT/OUTPUT BUFFER	40 DIP	General purpose buffer for keyboards, displays etc.

BASIC COMPONENTS

A. CP1610: 16-Bit Single-Chip Microprocessor

FEATURES

- 8 program accessible 16-bit general purpose registers
- 87 basic instructions
- 4 addressing modes: immediate, direct, indirect, relative
- Conditional branching on status word and 16 external conditions
- Unlimited interrupt nesting and priority resolution
- 16-bit 2's complement arithmetic & logic
- Status word: carry, overflow, sign, zero
- Direct memory access (DMA) for high speed data transfer
- 64K memory access using all address modes
- TTL compatible/simple bus structure
- 1 μs cycle time, 2 MHz 2-phase clock

DESCRIPTION

The CP1610 is a compatible member of the Series 1600 Microprocessor products family. It is a complete, 16-bit, single chip, high speed MOS-LSI Microprocessor. The Series 1600 family is fabricated with General Instrument's N-Channel Ion-Implant GIANT II process, insuring high performance with proven reliability and production history. All members of the Series 1600 family, including Programmable Interface Controllers, Read Only Memories, and Random Access Read/Write Memories are fully compatible with the CP1610.

The Microprocessor has been designed for high speed data processing and real time applications. Typical applications include programmable TV games, home computer systems/ home information centers, programmable calculator systems, peripheral controllers, process controllers, intelligent terminals and instruments, data acquisition and digital communications processors, numerical control systems and many general purpose mini-computer applications.The Microprocessor can readily support a variety of peripheral equipment such as TTY, CRT display, tape reader/punch, A/D & D/A converter, keyboard, cassette tape, floppy disk, and RS-232C data communication lines.

The CP1610 utilizes third generation minicomputer architecture with eight general purpose registers to achieve a versatile, sophisticated microcomputer system. The 16-bit word enables fast and efficient processing of alphanumeric or byte oriented data. The 16-bit address capability permits access to 65,536 words in any combination of program, memory, data memory, or peripheral devices. This single address space concept, combined with a powerful instruction set and microprogrammable Peripheral Interface devices, provides an efficient solution to microcomputer and many minicomputer-based product requirements.

B. AY-3-8900/AY-3-8900-1: Standard Television Interface

FEATURES: FOREGROUND OBJECTS

- Eight truly general purpose objects
- Coordinate positioned 160 H by 96V
- Object drawn from programmable library (32 angles)
- Zoom facilities in X and Y
- Priority draw feature
- Full interaction logic

FEATURES: BACKGROUND OBJECTS

- 20 × 12 background matrix of 8 × 8 squares
- All 240 locations drawn from library
- Grouping facility for large objects
- Moving effect in X and Y to full resolution
- Background may be changed by microprocessor during draw sequence
- Colored squares feature 960 independently colored areas

DESCRIPTION

The STIC circuit is the video processor which fetches, decodes and displays moving and background characters stored in the library for T.V. presentation under program control. During active picture time, interactions between shapes are recorded for interrogation by the CP1610 on completion of the current frame. The picture generation of the STIC can be separated into the two areas of background objects and moving objects. In operation, the 240 words of background RAM are loaded as required during the active period of picture time and a special buffer area allows both the STIC and the CP1610 to run together. The control data for the eight moving objects is stored within the STIC itself and it is accessed by the CP1610 only during the frame flyback period. All data is statically held and only needs to be updated on a picture change. In addition to the moving object data, the STIC also stores the border color, the background offset for moving background effects and a four-deep cyclic stack of background colors. If the optional graphics RAM is also wired into the system, the CP1610 can access this area during the vertical retrace period via the system bus and some special STIC connections. An additional control code can extend the CPU time for system access as the program demands.

C. RO-3-9502: Program ROM

FEATURES

- 2048 × 10 bit ROM organization
- Address and data on single 16 bit tristate bus
- 5 bit programmable chip select
- Output address latches and control signals generated for controlling up to 65K of external RAM
- Internal address status and data bits latched
- TTL compatible I/O
- Single +5 Volt power supply
- Ideal for microprocessors with multiplexed I/O bus for address and data.
- Totally automated custom programming
- 16 bit programmable initialization and interrupt response addresses output to I/O bus

DESCRIPTION

The 20K program ROM is organized into 2048 10 bit words to control the CP1610 operation. In addition to the stored program function, the circuit contains a 16 bit latched output port which supplies an address bus to any standard memory circuits which may be added by the user. An example of this addition would be a buffer store for a cassette tape reader. The program also supplies enable and read/write signals for the standard memory.

On master reset or for the end of active picture interrupt, the program ROM supplies the interrupt address to the CP1610.

D. RO-3-9503: Graphics ROM

FEATURES

- 2048 × 8 bit ROM organization
- Address and data on single 16 bit tristate bus
- 5 bit programmable chip select
- Output address latches and control signals generated for controlling up to 2K of external RAM
- Internal address status and data bits latched
- TTL compatible I/O
- Single +5 Volt power supply
- Ideal for microprocessors with multiplexed I/O bus for address and data.
- Totally automated custom programming
- 16 bit programmable initialization and interrupt response addresses output to I/O bus

DESCRIPTION

The 16K graphics ROM is a similar device to the program ROM, but is organized into 256 8×8 bit characters which are the dot patterns for background and moving objects. The set contains the full 64 character alpha-numeric and the other characters may be grouped by the user to have some program significance, although any character can be drawn in any mode.

The graphics ROM is accessed under two conditions, moving objects and background objects. For backgrounds, the RAM device sequentially outputs 14 bit words and 8 bits of this word defines one of the 256 stored characters. The STIC outputs a further 3 bits to define which line of the 8×8 bit matrix is being accessed. This 11 bit address is latched into the graphics ROM including a higher order bit which signifies if graphics ROM or RAM is to be accessed.

E. RA-3-9600: System RAM

FEATURES

- Sufficient memory storage to hold complete STIC background display (240 words of 14 bits).
- Sufficient memory storage to provide useful Scratch pad area for CP1610 microprocessor (112 words of 16 bits).
- Address latch for CP1610.
- Control decoder for CP1610.
- Address latch for STIC.
- Current line buffer for 8900 game system (20 words of 14 bits).

DESCRIPTION

The system RAM is an optimized structure device which allows maximum processor time for both game and graphics processors and it allows the user to run operational programs with only a single RAM package in the system. The RAM contains its own control decoding and address latch for both the CP1610 and the STIC. The two processors run on a semi-time shared basis with the RAM providing the data buffer.

The RAM is organized with 240 words holding the background picture data and 112 words being available to the CP1610 for general purpose scratchpad. The background storage area may be accessed by the CP1610 during the active picture time, which allows the user to run very complex, high density background displays.

OPTIONAL COMPONENTS

A. RO-3-9500: Cartridge ROM

The RO-3-9500 is a similar device to the RO-3-9502 Program ROM except that facilites for the control of external RAM are not provided. This allows for the packaging of this 20K ROM in a 28 pin DIP for use as a "satellite" or cartridge ROM for expansion of the 8900 system functions. A 40 lead 9502 may also be used in the "satellite" position if desired.

B. 2112/2114: Program/Graphics RAM

User-supplied standard RAMs, such as the 2112A (256 × 4) or 2114 (1K × 4), may be added to the 8900 system for use as either additional Program storage or Graphics RAM.

A typical use of expanded Program RAM would consist of the requirement for buffer memory for a tape cassette reader.

By adding RAM area to the graphics picture storage of the GIMINI 8900 system, this will allow the user to load and modify the dot pattern of the pictures under program control. Effects such as large background objects covering several 8 × 8 bit squares and individual background movement may be achieved with a graphics RAM system.

C. AY-3-8910: Programmable Sound Generator

The AY-3-8910 is a Large Scale Integrated Circuit that can produce a wide variety of complex sounds under software control. It is easily interfaced to most 8 and 16-bit microprocessors; however, it is optimally designed to directly connect to the CP1600 series of microprocessors. The flexibility of the AY-3-8910 makes it useful in applications such as music synthesis, sound effects, audible alarms, and FSK modems. In addition, once interfaced, the AY-3-8910 provides the microprocessor with two parallel 8-bit bi-directional data ports that are TTL compatible. The analog sound outputs can each provide 4 bits of logarithmic D/A conversion.

The AY-3-8910 is manufactured in the N-Channel Ion Implant process. Operation requires a single 5V supply, a 2 MHz TTL clock and a microprocessor controller such as the 1600 series.

D. AY-3-8915: Color Processor

The AY-3-8915 color processor is intended to be interfaced with the 8900 game system. The interface control is carried on a five wire bus where one line performs an option switch relative to the operation of the other four lines. The 8915 also provides a 3.58 MHz clock to the 8900 chip.

The effect of this "control" line is to produce two distinct operating modes. In mode one, the 8900 chip will be in the active line condition and attempting to draw some combination of background and foreground objects onto the telvision screen. The required color to be displayed is output from the 8900 on a four-line binary coded bus. This selects one from sixteen colors as defined by the game program being excecuted within the 8900 system.

With the control line in the mode two position, the four line bus is used to carry synchronizing infromation from the 8900 to the 8915. The four wires carry composite sync, color burst, line blanking and frame blanking. The operation of the 8915 driving mode two is such that the lines are decoded by the hardwired logic and then presented to a small ROM, which programs the correct level for each of the signals.

E. AY-3-8920: Tape Cassette Interface

The AY-3-8920 is intended to provide full interface and control signals between the 8900 system and a standard cassette drive.

F. IOB 1680: Input/Output Buffer

The IOB1680 is a byte oriented programmable input/output buffer which provides comprehensive interfacing facilities for the 8900 system with a minimum of additional components. The circuit is fabricated in General Instrument N-Channel Ion Implant GIANT II process insuring high performance. with proven reliability and production history.

The IOB1680 enables efficient interfacing between a peripheral and the CP1610 by the use of six 8-bit registers and a 16-bit programmable timer. Two of the 8-bit registers are a buffer store between the CP1610 and the bidirectional I/O lines to peripheral, latching any data sent to them from the CP1610. Three other 8-bit registers hold the Interrupt Vector Addresses associated with I/O, Error Status and the Timer. The Control Register governs the operation and characteristics of the IOB1680 and provides a convenient means for the CP1610 to monitor I/O status information. The 16-bit timer gives the IOB1680 a real time capability which is suitable for confirming system security and for timing peripheral activites. These registers are initialized after power clear by the CP1610 program writing the required Interrupt vector addresses into the appropriate registers. The interrupt vectors may also be altered at any time by program.

NORTH AMERICA

UNITED STATES:
GENERAL INSTRUMENT CORPORATION MICROELECTRONICS
HEADQUARTERS—600 West John Street, Hicksville, New York 11802
Tel: 516-733-3107. TWX: 510-221-1866

NORTHEAST—Riverside Office Park, Suite 103, Riverside Road, Weston, Massachusetts 02193
Tel: 617-899-8800. TWX: 710-324-0767

SOUTHEAST—383 Hillen Road, Towson, Maryland 21204
Tel: (301) 296-8010. TWX: 710-862-9083

EAST CENTRAL—200 Witmer Road, Box 346, Horsham, Pennsylvania 19044
Tel: (215) 674-4800. Telex: 831407

CENTRAL—3101 West Pratt Boulevard, Chicago, Illinois 60645
Tel: 312-338-9200. TWX: 910-221-1416

SOUTHWEST—2355 West Williams Field Road, Chandler, Arizona 85224
Tel: 602-963-7373. TWX: 910-950-1963

WESTERN—1100 Quail Street, Suite 114, Newport Beach, California 92660
Tel: 714-833-9400. TWX: 910-595-1730

ASIA

HONG KONG:
GENERAL INSTRUMENT HONG KONG LTD.
Room 704, Star House, 3 Salisbury Road, Kowloon
Tel: 3-675528. Telex: 84606

JAPAN:
GENERAL INSTRUMENT INTERNATIONAL CORP.
Fukide Bldg., 8th floor, 1—13 Toranomon 4-Chome
Minato-ku, Tokyo 105
Tel: (03) 437-0281. Telex: 26579

TAIWAN:
GENERAL INSTRUMENT MICROELECTRONICS TAIWAN
82—11 Kaohsiung Export Processing Zone, Kaohsiung
Tel: (07) 830402. Telex: 785-81901

EUROPE

EUROPEAN SALES HEADQUARTERS:
GENERAL INSTRUMENT MICROELECTRONICS LTD.
Regency House, 1—4 Warwick Street, London W1R 5WB
Tel: 01-439 1891. Telex: 23272

CENTRAL EUROPEAN SALES OFFICE:
GENERAL INSTRUMENT DEUTSCHLAND GmbH
(MOS Produktgruppe)
Nordendstrasse 3, 8000 Munchen 40
Tel: (089) 28.40.31. Telex: 528054

SOUTHERN EUROPEAN SALES OFFICE:
Via Lorenzetti 6, 20100 Milano
Tel: 02/4084101. Telex: 39423

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